Dedication

To my student

To my parent

To my family

In memory of my grand father, Al haja Battol

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First, I would like to thank my supervisor, professor: Abd Alrasol Jabar Alzubaidy for his guidance, patience, and information in achieving this research. I attribute this thesis degree to his expert advice and encouragement; without him, completion of this thesis would not have been possible.

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Abstract

The thesis has introduced a Digital Systems Design Using Computer Aided Design (DSDUCAD) tool, which is the process of simulation software that models the behavior of a circuit containing any mix of digital devices and download software which down load the design into the PLD, which mentioned as top down design methodology.

The main objective of this thesis is to design and simulate digital system using CAD tools. For this purpose, digital system modules were designed using MAX+PLUSII software. VHDL is used to write a code to describe the structure of a module using three examples of (a decoder, a multiplexer and a full-adder).A simulation for these modules, is also performed to obtain the result. Furthermore the design files were loaded to the CPLD chip through the serial port of the PC, using a download software (DNL82). Also the designs were tested and found the same results were obtained.

التجريد

فى هذا البحث شملت الدراسة تصميم النظم الرقمية بمساعدة أدوات الحاسب الألى DSDCAD Tools

Top down(التى تشمل تمثيل برامج المحاكاة بالحاسوب لنمذجت سلوكيات الدوائر الرقمية , و تشمل ايضا برمجت وحدات المنطق القابلة للبرمجة (ما يسمى بالتصميم من اعلى الى اسفل design

حيث تمت VHDL يهف البحث الى تصميم و محاكاة النظم الرقمية بمساعد الحاسب الالى , و لهذا الغرض تم تصميم نماذج للنظم الرقمية باستخدام برنامج ماكس+تو MAX+PLUSIIكتابة الكود بلغة الـ

لثلاثة أمثله مختلفه هي(decoder, Multiplexer and Full Adder)ثم تم تطوير فى كتابة البرنامج.

واعطى تطوير البرامج نتائج من خلال هذا البرنامج . كما تم إستخدام برنامج DNL82لبرمجة الشريحة

. من خلال منفذ الادخل و الاخراج التسلسلى . تم إختبار التصميم الجديد على لوحة اختبار , واعطى نتائج مشابه لعملية المحاكاه

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NOMENCLATURE

ABEL	Advanced Binary Expression Language
AHDL	Altera Hardware Description Language
AHPL	Altera Hardware Programming Language
ASIC	Application Specific Integrated Circuit
ACF	Assignment and Configuration File
CAD	Computer Aid Design
CAE	Computer Aided Engineering
CDL	Computer Design Language
CONLAN	Consensus Language
CPLD	Complex Programmable Logic Device
DSDUCAD*	Digital Systems Design Using CAD
EDA	Electronic Design Automation
FPGA	Field Programmable Gate Array
HDL	Hardware Description Language
MSI	Medium Scale Integration
PAL	Programmable Array Logic
PLD	Programmable Logic Device
VHSIC	Very high speed integrated circuit
VHDL	VHSIC Hardware Description Language
UP	University Program
UP1	UP education board
ISPS	Instruction Set Processor Specification
IC	Integrate Circuit
IDL	Interactive Design Language
TEGAS	Test Generation And Simulation

- this abbreviation from owns my self

TI-HDL	Texas Instruments Hardware Description Language
SSI	Small Scale Integration
SOC	System On Chip
SNF	Simulator Netlist File
RPT	Report File
Fit	Fit file