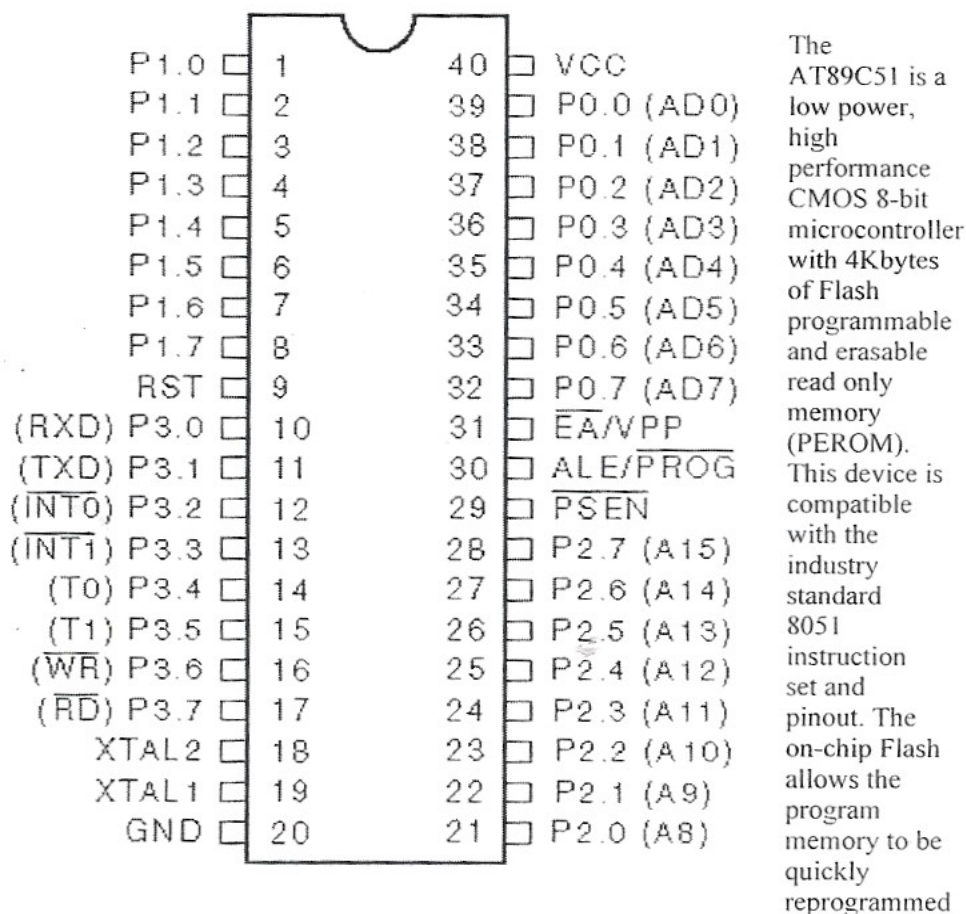


Appendix A

ATMEL AT89C51 Pinout and Description



using a nonvolatile memory programmer such as the PG302 (with the ADT87 adapter). By combining an industry standard 8-bit CPU with Flash on a monolithic chip, the 8951 is a powerful microcomputer which provides a highly flexible and cost effective solution to many embedded control applications. The 8951 provides the following features:

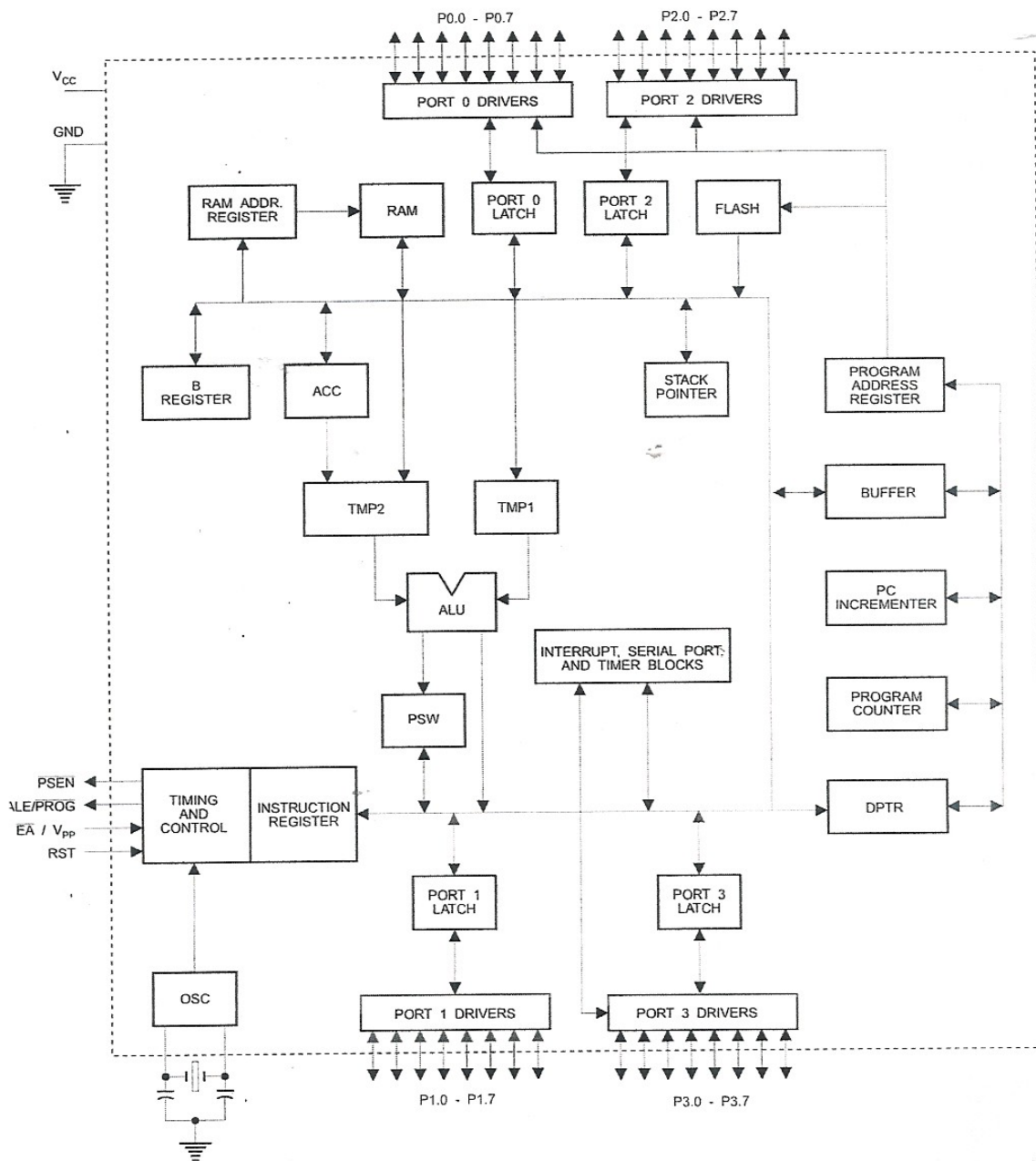
- ~ 4 Kbytes of Flash
- ~ 128 bytes of RAM
- ~ 32 I/O lines
- ~ two 16-bit timer/counters
- ~ five vector, two-level interrupt architecture
- ~ full duplex serial port
- ~ on chip oscillator and clock circuitry

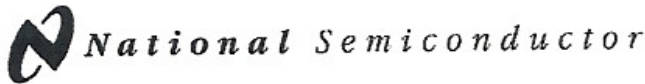
In addition, the 8951 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The Power Down Mode saves the RAM contents but freezes the oscillator disabling all other chip functions until the next hardware reset.

For more information on the PG302 Programmer and the ADT87 Adapter, click here.



Block Diagram





December 1994

ADC0801/ADC0802/ADC0803/ADC0804/ADC0805 8-Bit μ P Compatible A/D Converters

General Description

The ADC0801, ADC0802, ADC0803, ADC0804 and ADC0805 are CMOS 8-bit successive approximation A/D converters that use a differential potentiometric ladder—similar to the 256R products. These converters are designed to allow operation with the NSC800 and INS8080A derivative control bus with TRI-STATE® output latches directly driving the data bus. These A/Ds appear like memory locations or I/O ports to the microprocessor and no interfacing logic is needed.

Differential analog voltage inputs allow increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

Features

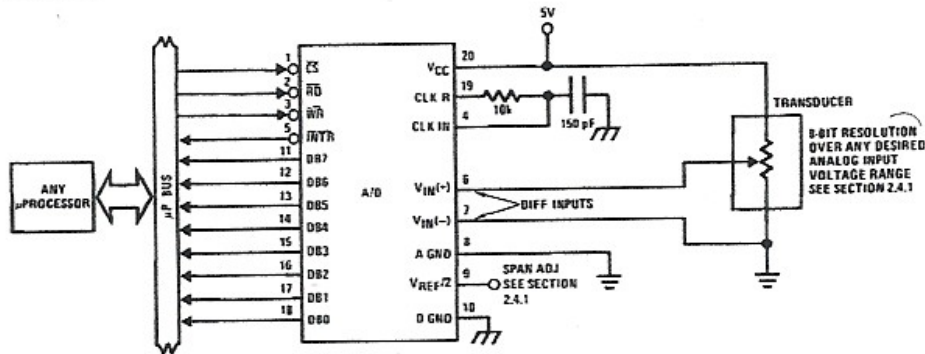
- Compatible with 8080 μ P derivatives—no interfacing logic needed - access time - 135 ns
- Easy interface to all microprocessors, or operates "stand alone"

- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- No zero adjust required
- 0.3" standard width 20-pin DIP package
- 20-pin molded chip carrier or small outline package
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference

Key Specifications

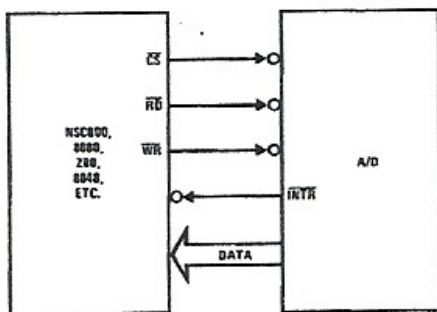
- Resolution 8 bits
- Total error $\pm 1/4$ LSB, $\pm 1/2$ LSB and ± 1 LSB
- Conversion time 100 μ s

Typical Applications



TL/H/5671-1

8080 Interface



TL/H/5671-31

Error Specification (Includes Full-Scale, Zero Error, and Non-Linearity)

Part Number	Full-Scale Adjusted	V _{REF/2} = 2.500 V _{DC} (No Adjustments)	V _{REF/2} = No Connection (No Adjustments)
ADC0801	$\pm 1/4$ LSB		
ADC0802		$\pm 1/2$ LSB	
ADC0803	$\pm 1/2$ LSB		
ADC0804		± 1 LSB	
ADC0805			± 1 LSB

TRI-STATE® is a registered trademark of National Semiconductor Corp.
Z-60® is a registered trademark of Zilog Corp.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage	
Logic Control Inputs	-0.3V to +18V
At Other Input and Outputs	-0.3V to ($V_{CC} + 0.3V$)
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

Storage Temperature Range	-65°C to +150°C
Package Dissipation at $T_A = 25^\circ\text{C}$	875 mW
ESD Susceptibility (Note 10)	800V

Operating Ratings (Notes 1 & 2)

Temperature Range	$T_{MIN} \leq T_A \leq T_{MAX}$
ADC0801/02LJ, ADC0802LJ/883	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$
ADC0801/02/03/04LCJ	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$
ADC0801/02/03/05LCN	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$
ADC0804LCN	$0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$
ADC0802/03/04LCV	$0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$
ADC0802/03/04LCWM	$0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$
Range of V_{CC}	4.5 V_{CC} to 6.3 V_{CC}

Electrical Characteristics

The following specifications apply for $V_{CC} = 5 V_{CC}$, $T_{MIN} \leq T_A \leq T_{MAX}$ and $f_{CLK} = 640 \text{ kHz}$ unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
ADC0801: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			$\pm 1/4$	LSB
ADC0802: Total Unadjusted Error (Note 8)	$V_{REF}/2 = 2.500 V_{CC}$			$\pm 1/2$	LSB
ADC0803: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			$\pm 1/2$	LSB
ADC0804: Total Unadjusted Error (Note 8)	$V_{REF}/2 = 2.500 V_{CC}$			± 1	LSB
ADC0805: Total Unadjusted Error (Note 8)	$V_{REF}/2$ No Connection			± 1	LSB
$V_{REF}/2$ Input Resistance (Pin 9)	ADC0801/02/03/05 ADC0804 (Note 9)	2.5 0.75	8.0 1.1		k Ω k Ω
Analog Input Voltage Range	(Note 4) $V_I(+)$ or $V_I(-)$	Ground-0.05		$V_{CC} + 0.05$	V_{CC}
DC Common-Mode Error	Over Analog Input Voltage Range		$\pm 1/4$	$\pm 1/2$	LSB
Power Supply Sensitivity	$V_{CC} = 5 V_{CC} \pm 10\%$ Over Allowed $V_{IN}(+)$ and $V_{IN}(-)$ Voltage Range (Note 4)		$\pm 1/4$	$\pm 1/2$	LSB

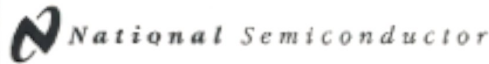
AC Electrical Characteristics

The following specifications apply for $V_{CC} = 5 V_{CC}$ and $T_A = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_C	Conversion Time	$f_{CLK} = 640 \text{ kHz}$ (Note 6)	103		114	μs
T_C	Conversion Time	(Note 5, 6)	66		73	$1/f_{CLK}$
f_{CLK}	Clock Frequency Clock Duty Cycle	$V_{CC} = 5V$, (Note 5) (Note 5)	100 40	640	1460 60	kHz %
CR	Conversion Rate in Free-Running Mode	INTR sed to WR with $\overline{CS} = 0 V_{CC}$, $f_{CLK} = 640 \text{ kHz}$	8770		9708	conv/s
$t_{W(WR)}$	Width of WR Input (Start Pulse Width)	$\overline{CS} = 0 V_{CC}$ (Note 7)	100			ns
t_{ACC}	Access Time (Delay from Falling Edge of RD to Output Data Valid)	$C_L = 100 \text{ pF}$		135	200	ns
$t_{RST} - t_{RST}$	TRI-STATE Control (Delay from Rising Edge of RD to Hi-Z State)	$C_L = 10 \text{ pF}$, $R_L = 10k$ (See TRI-STATE Test Circuits)		125	200	ns
$t_{W} - t_{RST}$	Delay from Falling Edge of WR or RD to Reset of INTR			300	450	ns
C_{IN}	Input Capacitance of Logic Control Inputs			5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance (Data Buffers)			5	7.5	pF

CONTROL INPUTS (Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately)

$V_{IH}(1)$	Logical "1" Input Voltage (Except Pin 4 CLK IN)	$V_{CC} = 5.25 V_{CC}$	2.0		15	V_{CC}
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January 1995

DAC0808/DAC0807/DAC0806 8-Bit D/A Converters

General Description

The DAC0808 series is an 8-bit monolithic digital-to-analog converter (DAC) featuring a full scale output current settling time of 150 ns while dissipating only 33 mW with $\pm 5V$ supplies. No reference current (I_{REF}) trimming is required for most applications since the full scale output current is typically ± 1 LSB of $255 I_{REF}/256$. Relative accuracies of better than $\pm 0.19\%$ assure 8-bit monotonicity and linearity while zero level output current of less than $4 \mu A$ provides 8-bit zero accuracy for $I_{REF} \geq 2$ mA. The power supply currents of the DAC0808 series are independent of bit codes, and exhibits essentially constant device characteristics over the entire supply voltage range.

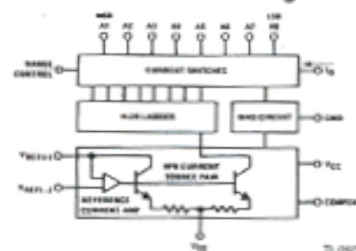
The DAC0808 will interface directly with popular TTL, OTL or CMOS logic levels, and is a direct replacement for the

MC1508/MC1408. For higher speed applications, see DAC0800 data sheet.

Features

- Relative accuracy: $\pm 0.19\%$ error maximum (DAC0808)
- Full scale current match: ± 1 LSB typ
- 7 and 6-bit accuracy available (DAC0807, DAC0806)
- Fast settling time: 150 ns typ
- Noninverting digital inputs are TTL and CMOS compatible
- High speed multiplying input slew rate: 8 mA/ μs
- Power supply voltage range: $\pm 4.5V$ to $\pm 18V$
- Low power consumption: 33 mW @ $\pm 5V$

Block and Connection Diagrams



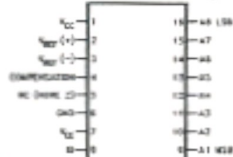
Order Number
DAC0808, DAC0807,
or DAC0806
See NS Package
Number J16A,
M16A or N16A

Dual-In-Line Package



TL/H15607-1

Small-Outline Package



Top View

TL/H15607-12

Ordering Information

ACCURACY	OPERATING TEMPERATURE RANGE	ORDER NUMBERS			
		J PACKAGE (J16A)*		N PACKAGE (N16A)*	
7-bit	$0^\circ C \leq T_{AS} \leq +75^\circ C$	DAC0807LCJ	MC1408L7	DAC0808LCN	MC1408P8
6-bit	$0^\circ C \leq T_{AS} \leq +75^\circ C$	DAC0806LCJ	MC1408L6	DAC0807LCN	MC1408P7
				DAC0806LCN	MC1408P6

*Note: Devices may be ordered by using either order number.



August 2005

LM340/LM78XX Series 3-Terminal Positive Regulators

General Description

The LM140/LM340A/LM340/LM78XXC monolithic 3-terminal positive voltage regulators employ internal current-limiting, thermal shutdown and safe-area compensation, making them essentially indestructible. If adequate heat sinking is provided, they can deliver over 1.0A output current. They are intended as fixed voltage regulators in a wide range of applications including local (on-card) regulation for elimination of noise and distribution problems associated with single-point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents.

Considerable effort was expended to make the entire series of regulators easy to use and minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply.

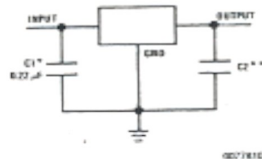
The 5V, 12V, and 15V regulator options are available in the steel TO-3 power package. The LM340A/LM340/LM78XXC series is available in the TO-220 plastic power package, and the LM340-5.0 is available in the SOT-223 package, as well as the LM340-5.0 and LM340-12 in the surface-mount TO-263 package.

Features

- Complete specifications at 1A load
- Output voltage tolerances of $\pm 2\%$ at $T_J = 25^\circ\text{C}$ and $\pm 4\%$ over the temperature range (LM340A)
- Line regulation of 0.01% of V_{OUT}/V of ΔV_{IN} at 1A load (LM340A)
- Load regulation of 0.3% of V_{OUT}/A (LM340A)
- Internal thermal overload protection
- Internal short-circuit current limit
- Output transistor safe area protection
- P* Product Enhancement tested

Typical Applications

Fixed Output Regulator

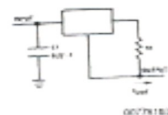


00778101

*Required if the regulator is located far from the power supply filter.

**Although no output capacitor is needed for stability, it does help transient response. (If needed, use 0.1 µF, ceramic disc).

Current Regulator

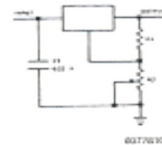


00778102

$$I_{OUT} = \frac{V_{Z3}}{R1} \approx I_Q$$

$I_Q = 1.3 \text{ mA}$ over line and load changes.

Adjustable Output Regulator

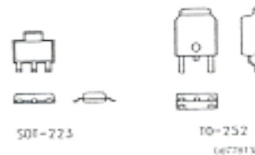


00778103

$$V_{OUT} = 5V + (5V/R1 + I_Q) R2 \quad 5V/R1 > 3 I_Q$$

$$\text{load regulation } (L_r) = [(R1 + R2)/R1] (L_r \text{ of LM340-5})$$

Comparison between SOT-223 and D-Pak (TO-252) Packages



Scale 1:1



August 2000

LM741 Operational Amplifier

LM741 Operational Amplifier

General Description

The LM741 series are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439 and 748 in most applications. The amplifiers offer many features which make their application nearly foolproof: overload protection on the input and

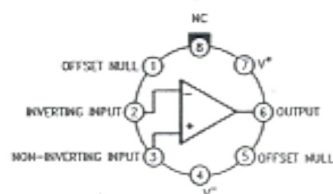
output, no latch-up when the common mode range is exceeded, as well as freedom from oscillations.

The LM741C is identical to the LM741/LM741A except that the LM741C has their performance guaranteed over a 0°C to +70°C temperature range, instead of -55°C to +125°C.

Features

Connection Diagrams

Metal Can Package

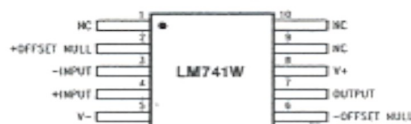


00034102

Note 1: LM741B is available per JMOB510/10101

Order Number LM741H, LM741H/883 (Note 1),
LM741AH/883 or LM741CH
See NS Package Number H08C

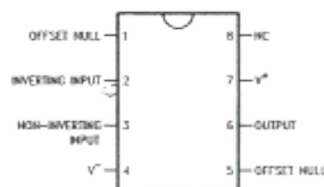
Ceramic Flatpak



00034106

Order Number LM741W/883
See NS Package Number W10A

Dual-In-Line or S.O. Package

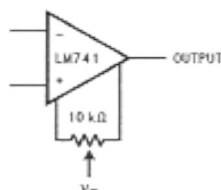


00034103

Order Number LM741J, LM741J/883, LM741CN
See NS Package Number J08A, M08A or N08E

Typical Application

Offset Nulling Circuit



00034107

Appendix F



March 1998

DM74LS47 BCD to 7-Segment Decoder/Driver with Open-Collector Outputs

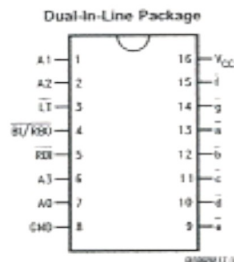
General Description

The LS47 accepts four lines of BCD (8421) input data, generates their complements internally and decodes the data with seven AND/OR gates having open-collector outputs to drive indicator segments directly. Each segment output is guaranteed to sink 24 mA in the ON (LOW) state and withstand 15V in the OFF (HIGH) state with a maximum leakage current of 250 μ A. Auxiliary inputs provided blanking, lamp test and cascadable zero-suppression functions.

Features

- Open-collector outputs
- Drive indicator segments directly
- Cascadable zero-suppression capability
- Lamp test input

Connection Diagram



Order Number DM54LS47J, DM54LS47W,
DM74LS47M or DM74LS47N
See Package Number J16A, M16A, N16E or W16A

Pin Names	Description
A0-A3	BCD Inputs
RBI	Ripple Blanking Input (Active LOW)
LT	Lamp Test Input (Active LOW)
BI/RBO	Blanking Input (Active LOW) or Ripple Blanking Output (Active LOW)
a - g	*Segment Outputs (Active LOW)

Note 1: *OC—Open Collector

DM74LS47 BCD to 7-Segment Decoder/Driver with Open-Collector Outputs

Absolute Maximum Ratings (Note 2)

Supply Voltage

7V

DM54LS

-55°C to +125°C

Input Voltage

7V

DM74LS

0°C to +70°C

Storage Temperature Range

-65°C to +150°C

Operating Free Air Temperature Range

Recommended Operating Conditions

Symbol	Parameter	DM54LS47			DM74LS47			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{OH}	High Level Input Voltage	2			2			V
V_{OL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current $\bar{a} - \bar{g}$ @ 15V = V_{OH} (Note 3)			-50			-250	μA
I_{OH}	High Level Output Current $\overline{BI}/\overline{RBO}$						-50	μA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	-55		125	0		70	C

Note 2: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these levels. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 3: OFF state at $\bar{a}-\bar{g}$.

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

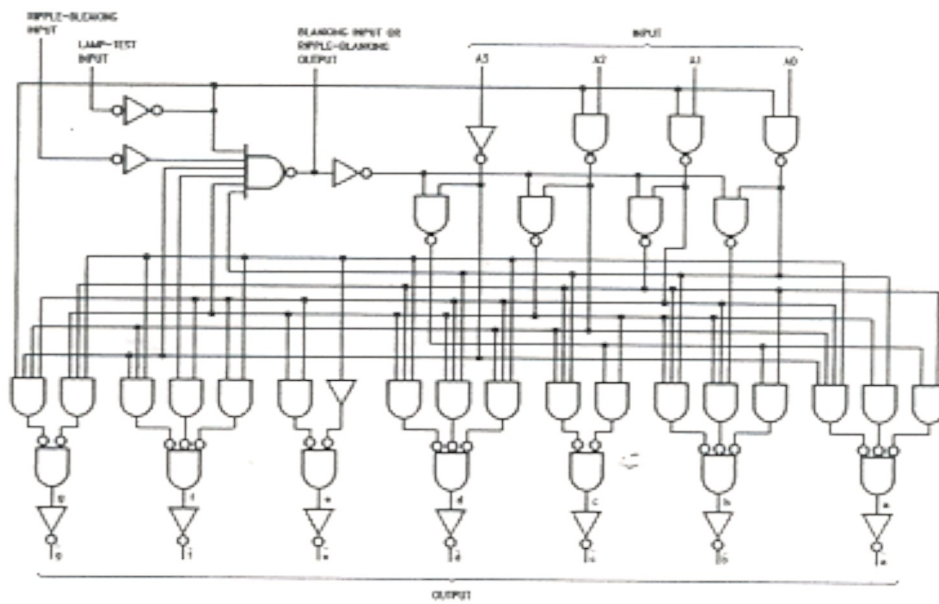
Symbol	Parameter	Conditions	Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	$V_{CC} = \text{Min}, I_I = -18 \text{ mA}$			-1.5	V
V_{OH}	High Level Output Voltage	$V_{CC} = \text{Min}, I_{OH} = \text{Max},$ $V_{OL} = \text{Max}, \overline{BI}/\overline{RBO}$	DM54 2.4 DM74 2.7	3.4		V
I_{OHP}	Output High Current Segment Outputs	$V_{CC} = 5.5V, V_O = 15V \bar{a} - \bar{g}$			250	μA
V_{OL}	Low Level Output Voltage	$V_{CC} = \text{Min}, I_{OL} = \text{Max},$ $V_{OH} = \text{Min}, \bar{a} - \bar{g}$	DM54	0.35	0.4	V
		$I_{OL} = 3.2 \text{ mA}, \overline{BI}/\overline{RBO}$	DM74		0.5	
		$I_{OL} = 12 \text{ mA}, \bar{a} - \bar{g}$	DM74	0.25	0.4	
		$I_{OL} = 1.6 \text{ mA}, \overline{BI}/\overline{RBO}$	DM74		0.4	
I_I	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}, V_I = 7V$ $V_{CC} = \text{Max}, V_I = 10V$	DM74 DM54		100	μA
I_{IH}	High Level Input Current	$V_{CC} = \text{Max}, V_I = 2.7V$			20	μA
I_{IL}	Low Level Input Current	$V_{CC} = \text{Max}, V_I = 0.4V$			-0.4	mA
I_{OS}	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 5), I_{OS} at $\overline{BI}/\overline{RBO}$	DM54 DM74	-0.3	-2.0	mA
I_{OC}	Supply Current	$V_{CC} = \text{Max}$			13	mA

Note 4: All typicals are at $V_{CC} = 5V, T_A = 25^\circ C$.

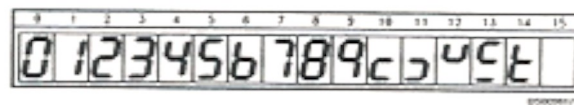
Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

F

Logic Diagram

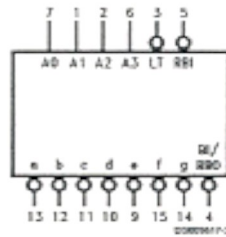


Numerical Designations—Resultant Displays



F

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

Truth Table

Decimal or Function	Inputs							Outputs							Note
	LT	RBI	A3	A2	A1	A0	BURBO	a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	(Note 7)
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	(Note 7)
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
$\overline{BI}$	X	X	X	X	X	X	L	H	H	H	H	H	H	H	(Note 8)
$\overline{RBI}$	H	L	L	L	L	L	L	H	H	H	H	H	H	H	(Note 9)
$\overline{LT}$	L	X	X	X	X	X	H	L	L	L	L	L	L	L	(Note 10)

Note 7: BURBO is wire-AND logic serving as blanking input ($\overline{BI}$) and/or ripple-blanking output ($\overline{RBO}$). The blanking out ($\overline{BI}$) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input ($\overline{RBI}$) must be open or at a HIGH level if blanking or a decimal 0 is not desired. X = input may be HIGH or LOW.

Note 8: When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a HIGH level regardless of the state of any other input condition.

Note 9: When ripple-blanking input ($\overline{RBI}$) and inputs A0, A1, A2 and A3 are LOW level, with the lamp test input at HIGH level, all segment outputs go to a HIGH level and the ripple-blanking output ($\overline{RBO}$) goes to a LOW level (response condition).

Note 10: When the blanking input/ripple-blanking output ($\overline{BURBO}$) is open or held at a HIGH level, and a LOW level is applied to lamp test input, all segment outputs go to a LOW level.



May 1989

DM54LS154/DM74LS154 4-Line to 16-Line Decoders/Demultiplexers

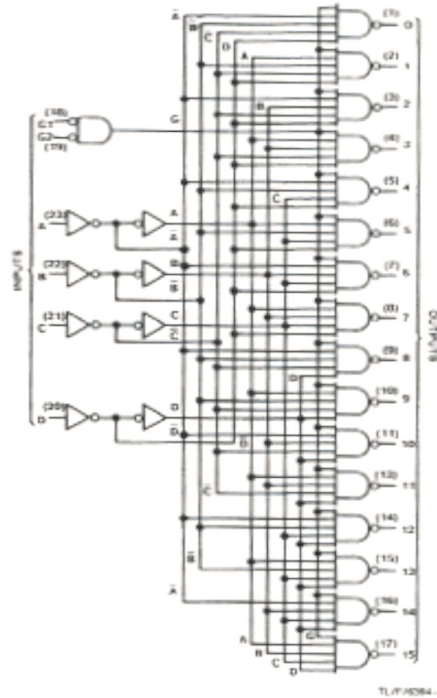
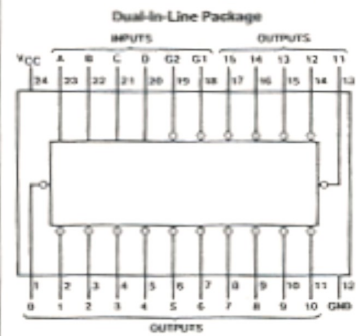
General Description

Each of these 4-line-to-16-line decoders utilizes TTL circuitry to decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs, G1 and G2, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high. These demultiplexers are ideally suited for implementing high-performance memory decoders. All inputs are buffered and input clamping diodes are provided to minimize transmission-line effects and thereby simplify system design.

Features

- Decodes 4 binary-coded inputs into one of 16 mutually exclusive outputs
- Performs the demultiplexing function by distributing data from one input line to any one of 16 outputs
- Input clamping diodes simplify system design
- High fan-out, low-impedance, totem-pole outputs
- Typical propagation delay
3 levels of logic 23 ns
Strobe 19 ns
- Typical power dissipation 45 mW

Connection and Logic Diagrams



Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	-55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	DM54LS154			DM74LS154			Units
		Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High Level Input Voltage	2			2			V
V _{IL}	Low Level Input Voltage			0.7			0.8	V
I _{OH}	High Level Output Current			-0.4			-0.4	mA
I _{OL}	Low Level Output Current			4			8	mA
T _A	Free Air Operating Temperature	-55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = -18 mA			-1.5	V
V _{OH}	High Level Output Voltage	V _{CC} = Min, I _{OH} = Max V _{IL} = Max, V _{IH} = Min	DM54 2.5	3.4		V
V _{OL}	Low Level Output Voltage	V _{CC} = Min, I _{OL} = Max V _{IL} = Max, V _{IH} = Min	DM54 DM74	0.25 0.35	0.4 0.5	V
I _I	Input Current @ Max Input Voltage	I _{OL} = 4 mA, V _{CC} = Min	DM74	0.25	0.4	mA
I _{IH}	High Level Input Current	V _{CC} = Max, V _I = 2.7V			20	μA
I _{IL}	Low Level Input Current	V _{CC} = Max, V _I = 0.4V			-0.4	mA
I _{OS}	Short Circuit Output Current	V _{CC} = Max (Note 2)	DM54 DM74	-20 -20	-100 -100	mA
I _{CC}	Supply Current	V _{CC} = Max (Note 3)		9	14	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R _L = 2 kΩ				Units
			C _L = 15 pF		C _L = 50 pF		
			Min	Max	Min	Max	
t _{PLH}	Propagation Delay Time Low to High Level Output	Data to Output		30		35	ns
t _{PHL}	Propagation Delay Time High to Low Level Output	Data to Output		30		35	ns
t _{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Output		20		25	ns
t _{PHE}	Propagation Delay Time High to Low Level Output	Strobe to Output		25		35	ns

Function Table																					
Inputs						Outputs															
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	L	H	L	H	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
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L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
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L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
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L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H

H = High Level, L = Low Level, X = Don't Care

Appendix H

276-058

FND 10

This device is a single digit readout module. It has highly legible bright red characters, uses low power (60mW), is IC compatible and is compact—12 digits in less than a 3" panel width.

Max Ratings:

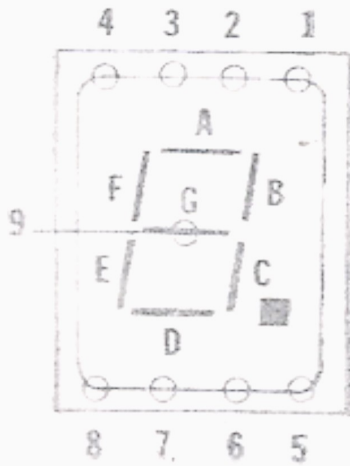
Reverse Voltage	3V
Dissipation/segment or decimal	20mW
Average Current/segment	10mA
Forward Voltage @ 5mA	1.65V (typ)

Electrical Characteristics (typical)

Intensity @ 5mA/segment	0.65mcd
Forward Voltage @ 10mA/segment	1.70V

Pin Connections

- Pin 1 Segment G
- Pin 2 Segment A
- Pin 3 Segment G
- Pin 4 Segment F
- Pin 5 Decimal
- Pin 6 Segment C
- Pin 7 Segment D
- Pin 8 Segment E
- Pin 9 Common Cathode



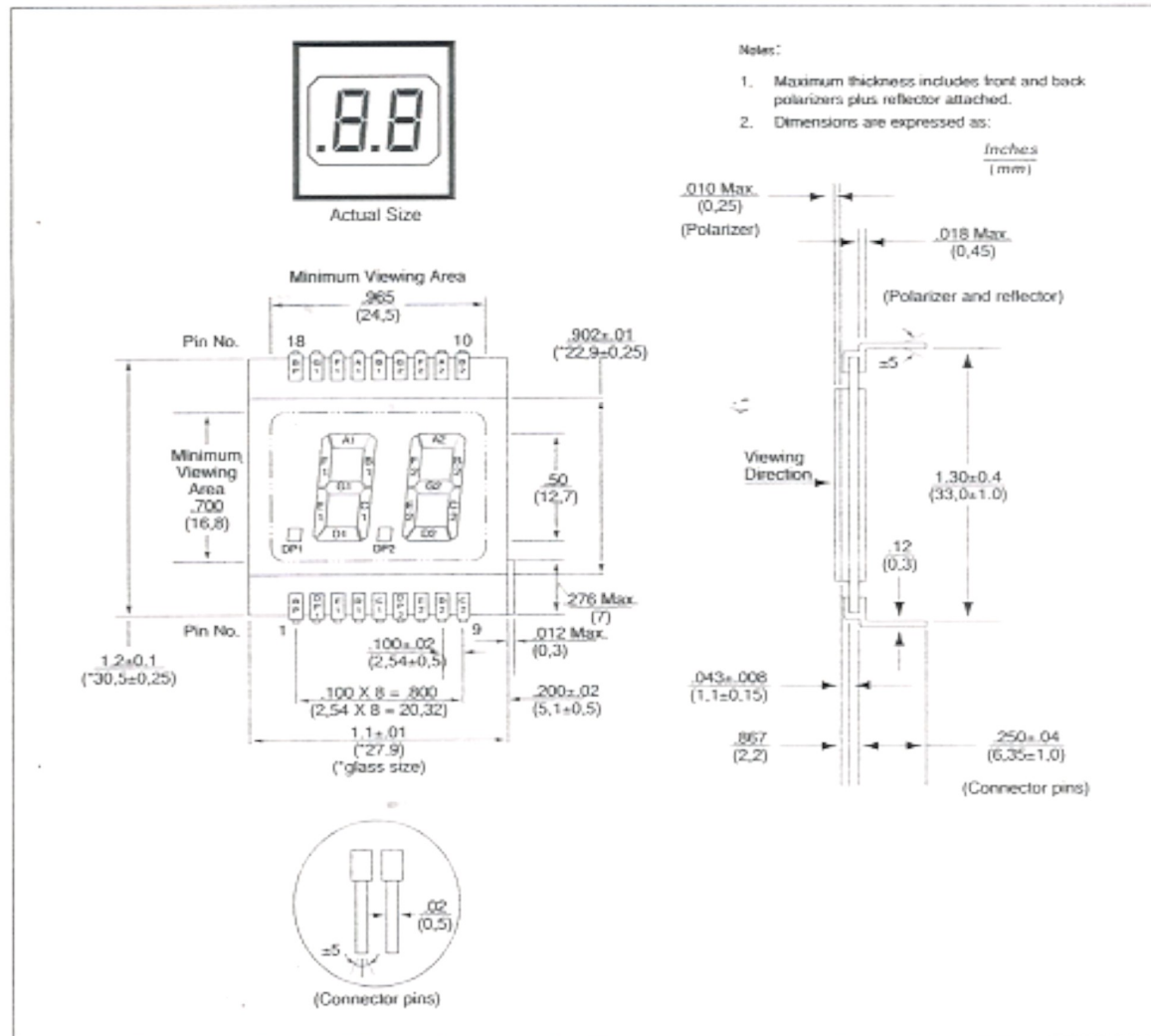
H

07/09/2005



FE1901 LCD Panel Display

FE1901 2 Digits, 0.5 Inch (12.7mm) Character Height



Pin Assignments

Pin #	Seg.	Pin #	Seg.	Pin #	Seg.	Pin #	Seg.	Pin #	Seg.	Pin #	Seg.	Pin #	Seg.	Pin #	Seg.	Pin #	Seg.
1	BP	3	E1	5	C1	7	E2	9	C2	11	A2	13	G2	15	A1	17	G1
2	DP1	4	D1	6	DP2	8	D2	10	B2	12	F2	14	B1	16	F1	18	BP

Product specifications contained herein may be changed without prior notice.
It is therefore advisable to contact Purdy Electronics before proceeding with the design of equipment incorporating this product.