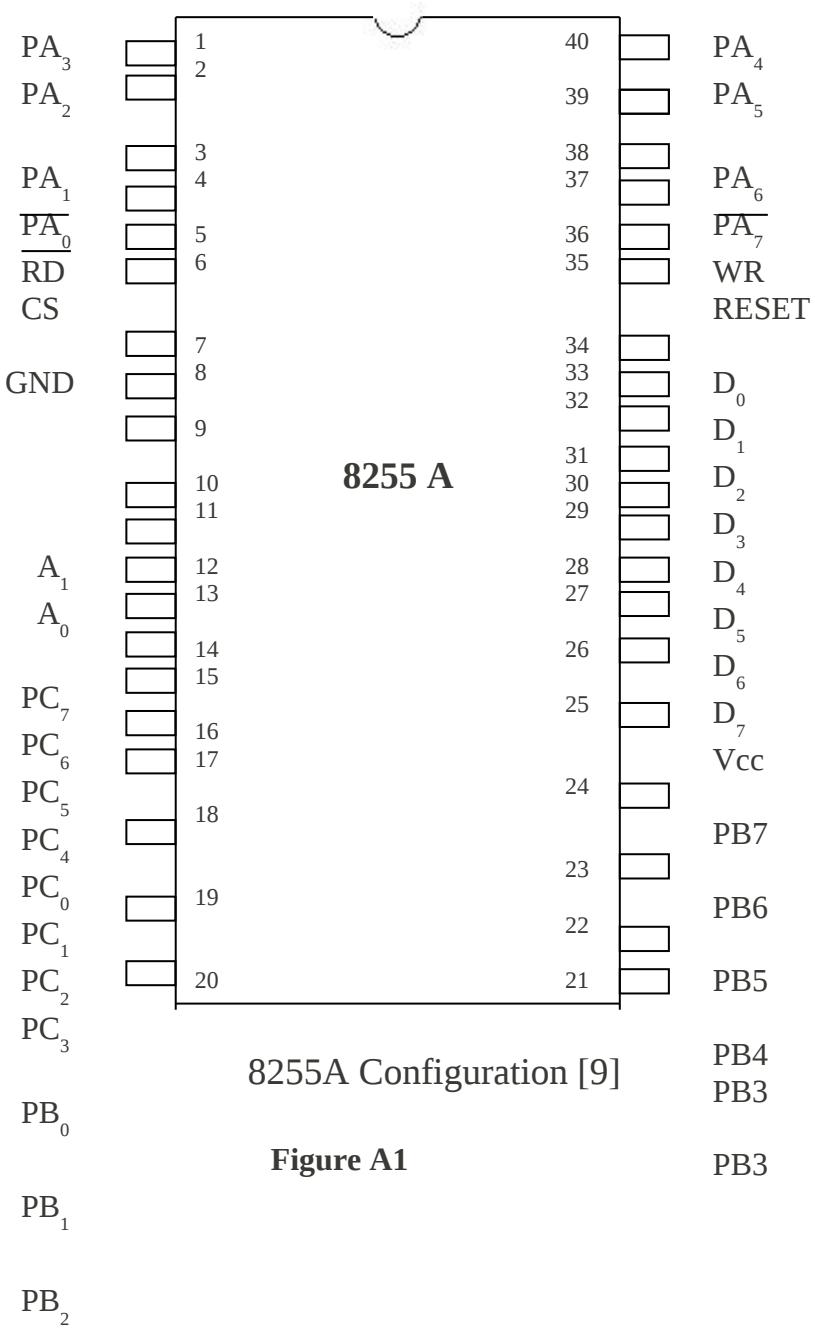
Appendix A: 8255A



8255A Configuration [9]

Figure A1

8255A
Electrical Specifications [9]

Vcc = 5.0 V ± 10%

Temp. Range: 0 ºC – 70 ºC

Symbol	Parameter	Limits		Units	Test Conditions
		Min	Max		
V_{IH}	Logical One Input Voltage	2.0 2.2	-	V	I 82C55A,C82C55A M82O55A
V_{IL}	Logical Zero Input Voltage	-	0.8	V	
V_{OH}	Logical One Output Voltage	3.0 $Vcc^{-0.4}$	-	V	I_{OH} = - 2.5 m A, I_{OH} = - 100 µA
V_{OL}	Logical Zero Output Voltage	-	0.4	V	I_{OL} = + 2.5 mA
I_{IN}	Input Leakage Current	- 1.0	- 1.0	µA	V_{IN} = Vcc or GND DIP Pins: 5, 6, 8, 9, 35, 36.
IO	I/O Pin Leakage Current	- 10	-10	µA	VO = Vcc or GND DIP Pins: 27 – 34
IBHH	Bus Hold High Current	- 50	-400	µA	VO = 3.0 V Port A, B, C
IBHL	Bus Hold Low Current	50	400	µA	VO = 1.0 V Port A ONLY
IDAR	Darlington Drive Current	-2.5	Note	mA	Ports A, B, C Test Condition 3
ICCSB	Standby Power Supply Current	-	10	µA	Vcc = 5.5 V. V_{IN} = Vcc or GND Output Open
ICCOP	Operating Power Supply Current	-	1	mA MHz	T_A = 25ºC. Vcc = 5.0 V. Typical.

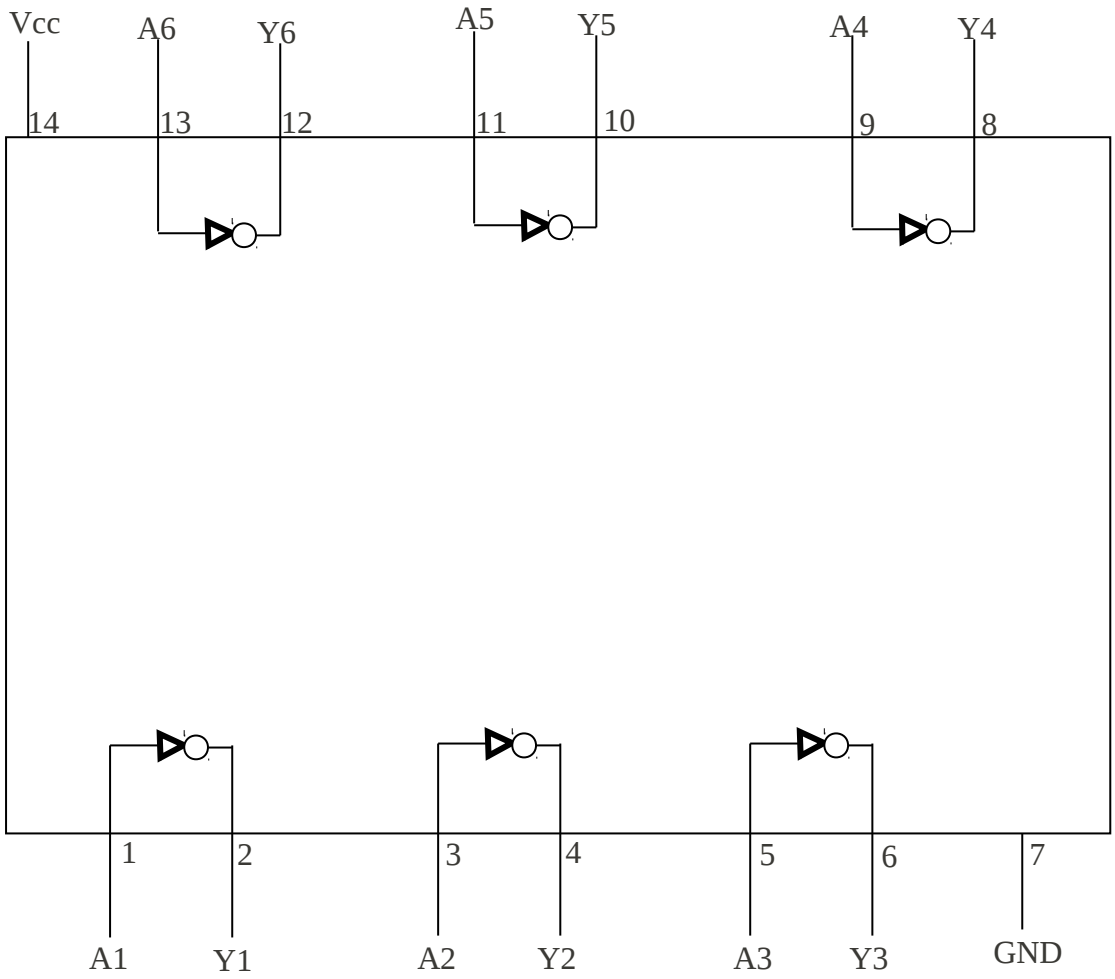
Note: No internal current limiting exists on port outputs. A resister must be added externally to limit the current.

Table A1

A2

Appendix B :MM47HC04

Dual-In-Line Package [8]



Top View

MM74HC04
Connection and Logic Diagrams

Figure B1

DC Electrical Characteristics of MM74HCO4 [8]

Hex-Inverter

MM74CO4

Vcc = 5 V ± 10%

Symbol	Parameter	Conditions	Vcc	T_A=25° C	74HC T_A=-40 to 85°C		Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High		2.0V		1.5	1.5	V
	Level Input		4.5V		3.15	3.15	V
	Voltage		6.0V		4.2	4.2	V
V_{IL}	Maximum Low		2.0V		0.5	0.5	V
	Level Input		4.5V		1.35	1.35	V
	Voltage		6.0V		1.8	1.8	V
V_{OH}	Minimum High	$V_{IN} = V_{IL}$					
	Level Output	$\|I_{OUT}20 \geq \|\mu A$	2.0V	2.0	1.9	1.9	V
	Voltage		4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		$V_{IN} = V_{IL}$					
		$\|I_{OUT}4.0 \geq \|mA$	4.5V	4.2	3.98	3.84	V
		$\|I_{OUT}5.2 \geq \|$ mA	6.0V	5.7	5.48	5.34	V
V_{OL}	Maximum Low	$V_{IN} = V_{IH}$					
	Level output	$\|I_{OUT}20 \geq \|\mu A$	2.0V	0	0.1	0.1	V
	Voltage		4.5V	0	0.1	0.1	V
			6.0V	0	0.1	0.1	V
		$V_{IN} = V_{IH}$					
		$\|I_{OUT}4.0 \geq \|mA$	4.5V	0.2	0.26	0.33	V
		$\|I_{OUT}5.2 \geq \|$ mA	6.0V	0.2	0.26	0.33	V
I_{IN}	Maximum Input	V_{IN} = Vcc or	6.0V		±0.1	±1.0	µA
	Current	GND					
I_{CC}	Maximum	V_{IN} = Vcc or	6.0V		2.0	20	µA
	Quiescent	GND					
	Supply Current	I_{OUT} = 0 µA					

Table B1

AC Electrical Characteristics Vcc = 2.0 V to 6.0 V
Of MM74HCO4 Hex Inverter [8]

MM74CO4

Symbol	Parameter	Conditions	Vcc	T_A=25° C	74HC T_A=-40 to 85°C		Units
				Typ	Guaranteed Limits		
t_{PHL} ,	Maximum		2.0V	55	95	120	ns
t_{PLH}	Propagation		4.5V	11	19	24	ns
	Delay		6.0V	9	16	20	ns
t_{TLH} ,	Maximum		2.0V	30	75	95	ns
t_{THL}	Output Rise and		4.5V	8	15	19	ns
	Fall Time		6.0V	7	13	16	ns
C_{PD}	Power	(per gate)		20			pF
	Dissipation						
	Capacitance						
C_{IN}	Maximum Input			5	10	10	pF
	Capacitance						

Table B2

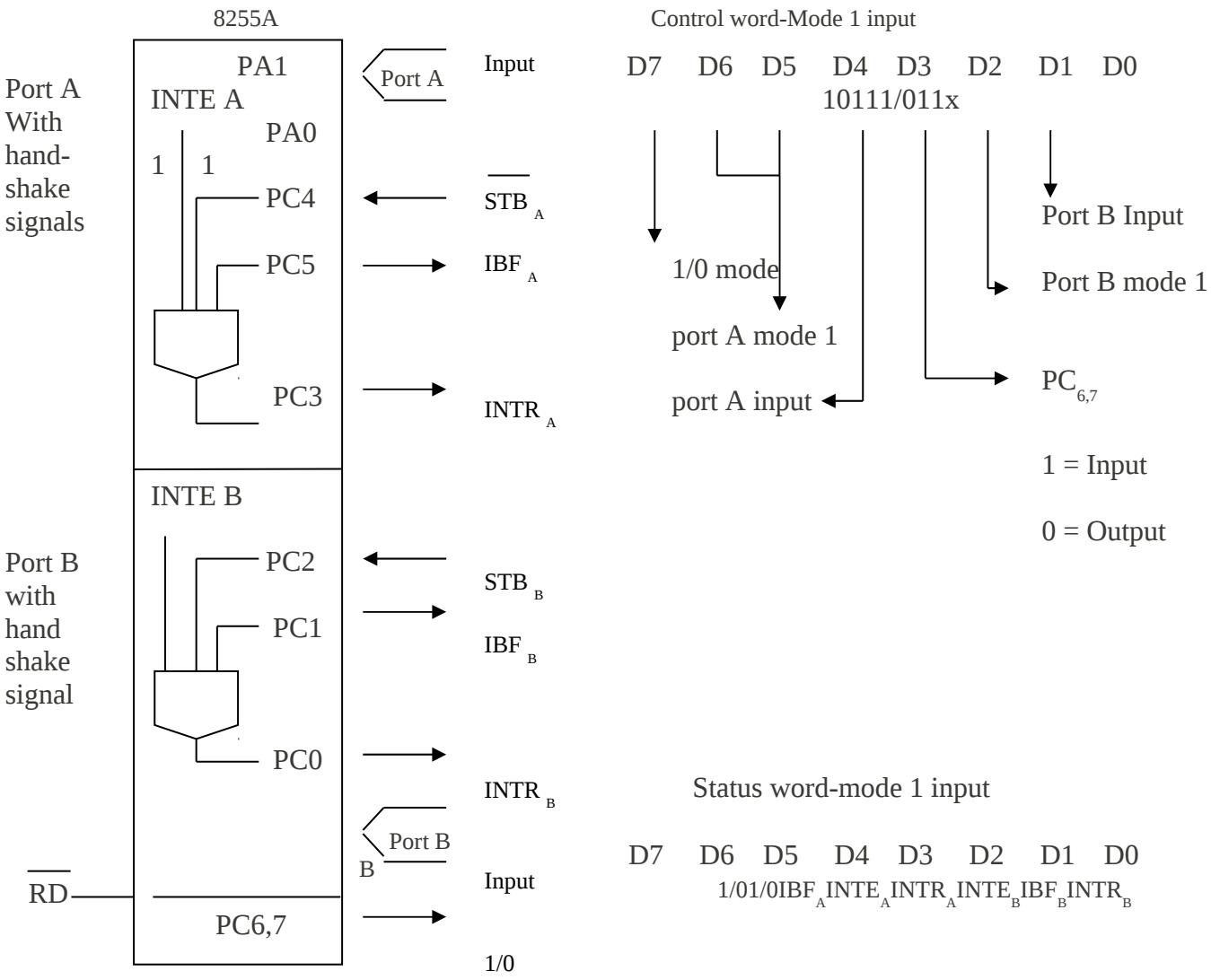
Appendix E :82C55A [9]

Mode Definition Summary

	Mode 0		Mode 1		Mode 2	
	IN	**OUT**	**IN**	**OUT**	**GROUP A ONLY**	
PA0	In	Out	In	Out	↔	
PA1	In	Out	In	Out	↔	
PA2	In	Out	In	Out	↔	
PA3	In	Out	In	Out	↔	
PA4	In	Out	In	Out	↔	
PA5	In	Out	In	Out	↔	
PA6	In	Out	In	Out	↔	
PA7	In	Out	In	Out	↔	
PB0	In	Out	In	Out		Mode 0 or Mode 1 Only
PB1	In	Out	In	Out		
PB2	In	Out	In	Out		
PB3	In	Out	In	Out		
PB4	In	Out	In	Out		
PB5	In	Out	In	Out		
PB6	In	Out	In	Out		
PB7	In	Out	In	Out		
PC0	In	Out	INTRB	INTRB	I/O	
PC1	In	Out	IBFB	OBFB	I/O	
PC2	In	Out	STBB	ACKB	I/O	
PC3	In	Out	INTRA	INTRA	INTRA	
PC4	In	Out	STBA	I/O	STBA	
PC5	In	Out	IBFA	I/O	IBFA	
PC6	In	Out	I/O	ACKA	ACKA	
PC7	In	Out	I/O	OBFA	OBFA	

Table E1

E1



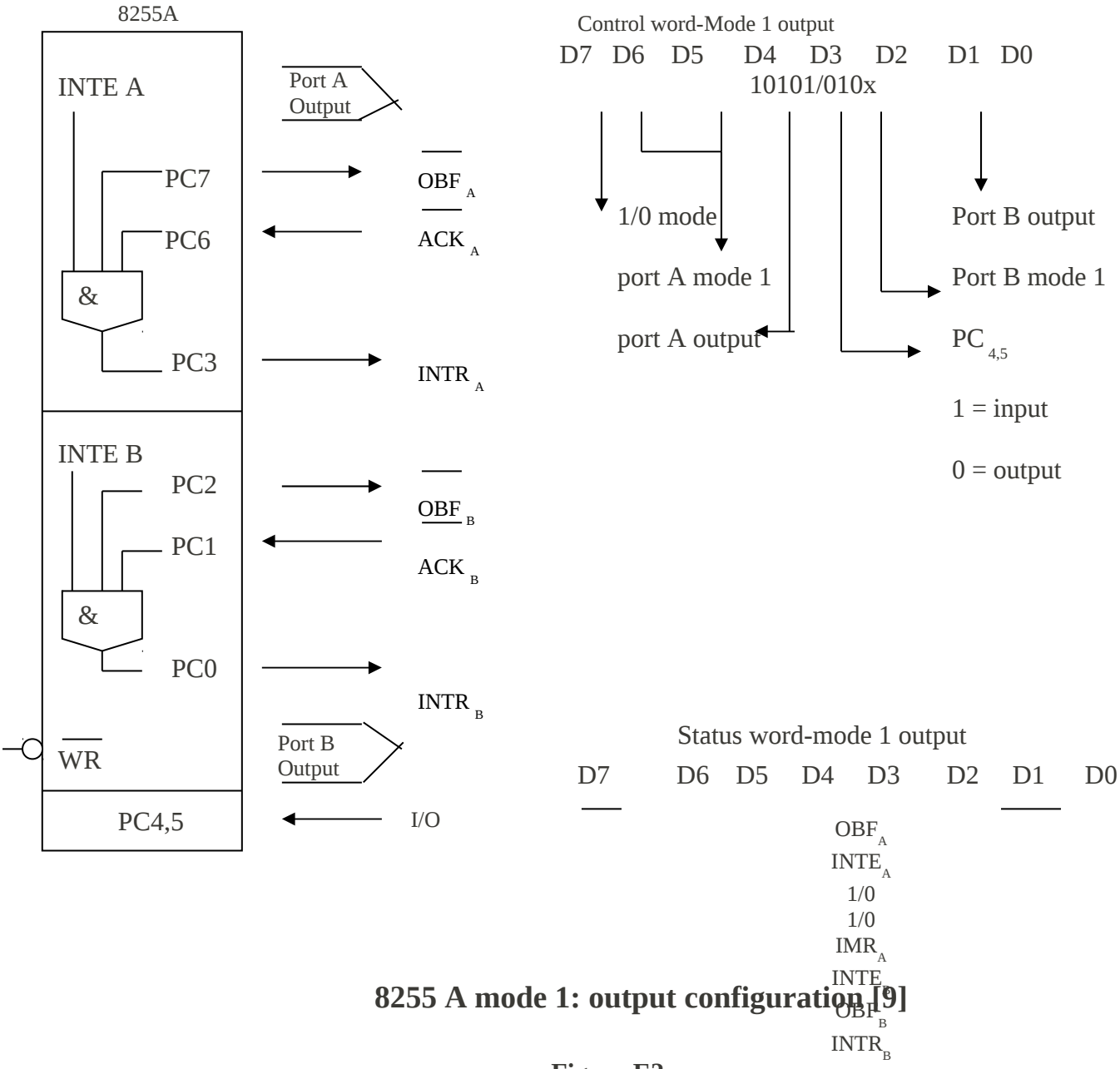
8255 A mode 1: input configuration [9]

Figure E1

Mode 1: input control signals [9]

Signal	Full name	Definition
STB	Strobe Input	It is active low, coming from peripheral device to indicate that it has transmitted a byte of data.
IBF	Input Buffer Full	It is generated by the MPU to indicate that the input latch has received the data byte.
INTR	Interrupt Request	It is an output signal that may be used to interrupt the MPU.
INTE	Interrupt Enable	This is an internal flip-flop used to enable or disable the INTR signal.

Table E2



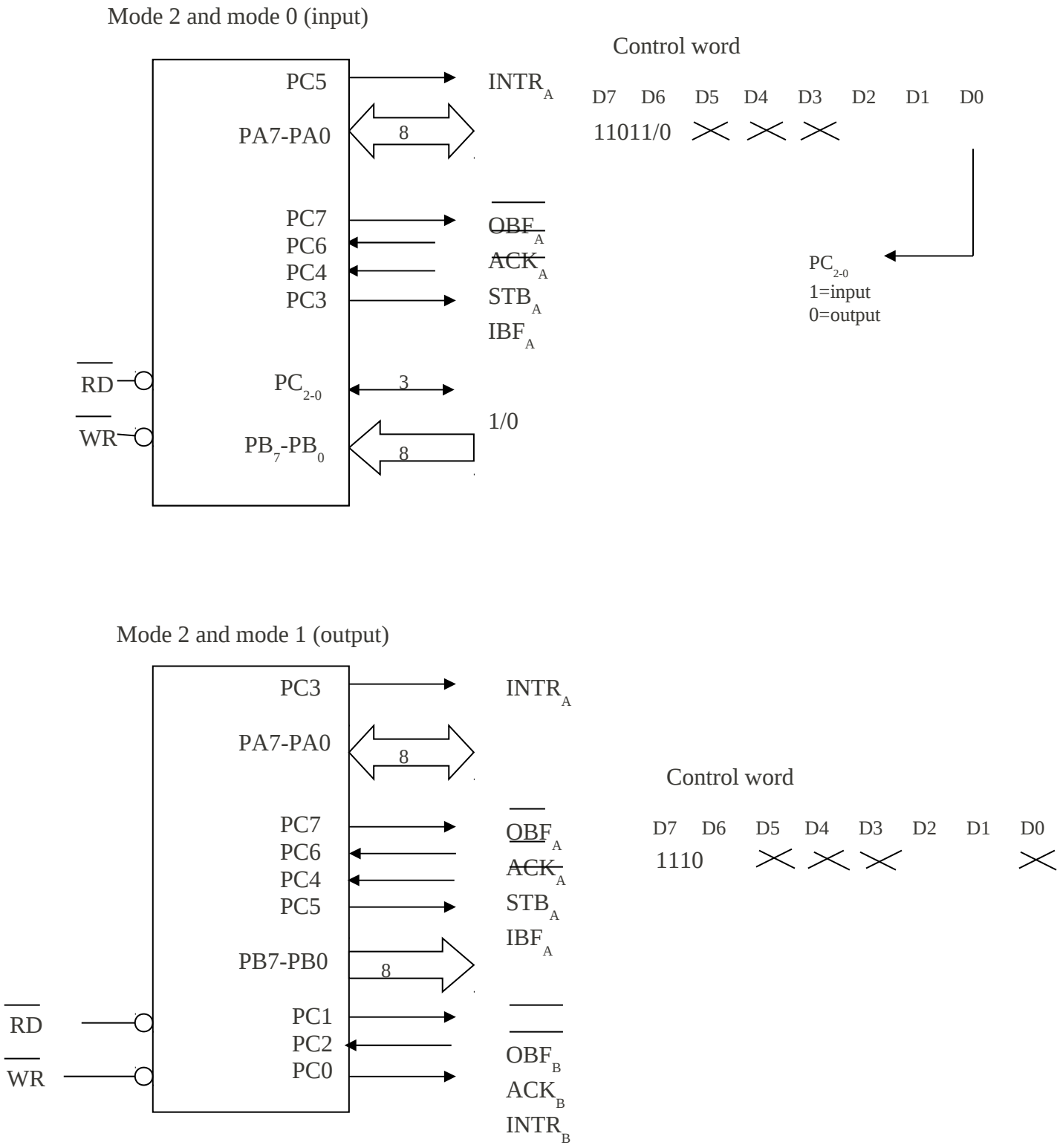
8255 A mode 1: output configuration [9]

Figure E2

Mode 1 Output control signals [9]

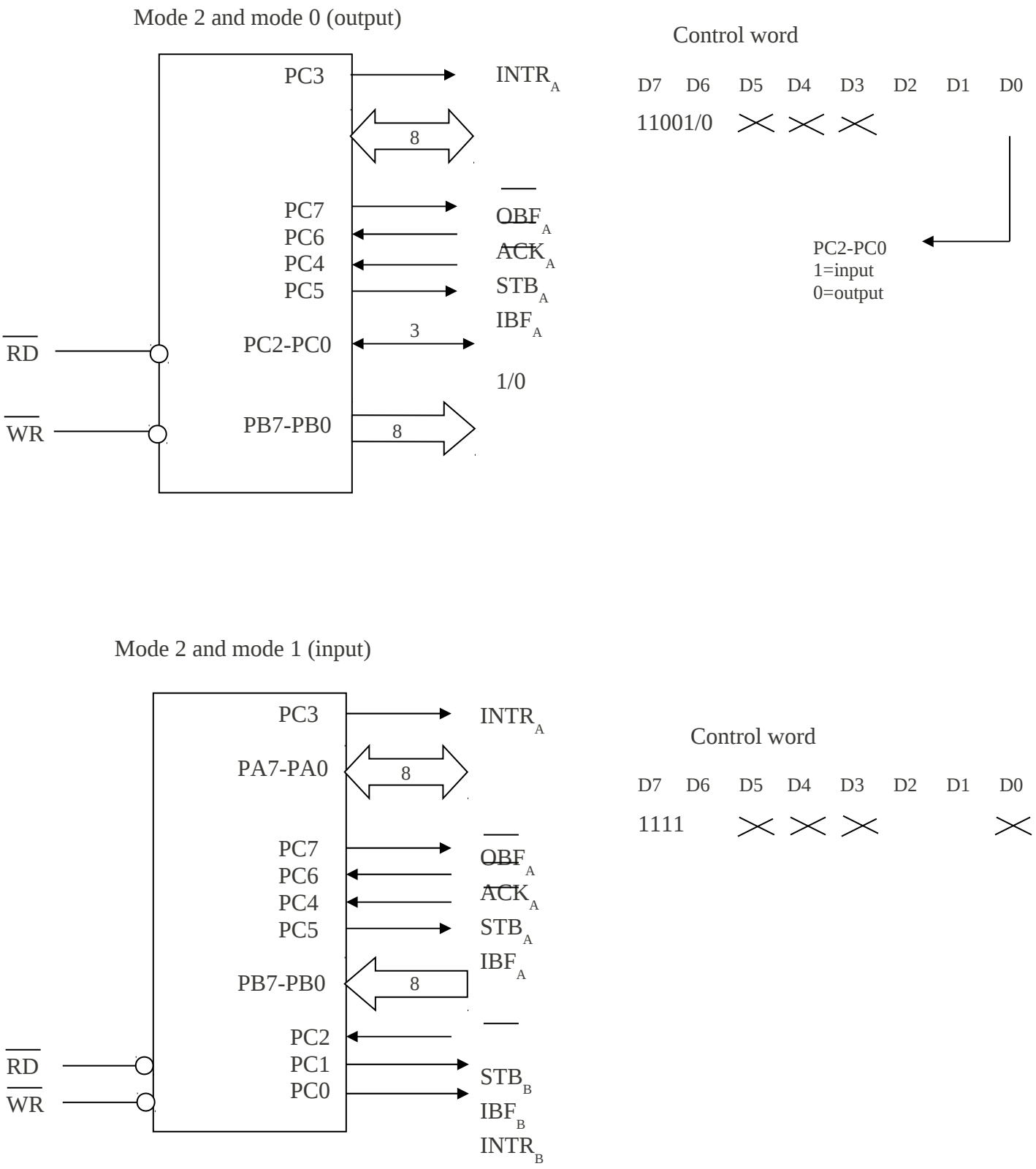
Signal	Full name	Definition
$\overline{OBF}$	Output Buffer Full	It is an output signal that goes low when the MPU writes data into the output latch of the 8255A. It indicates to an output peripheral that new data are ready to be read.
$\underline{ACK}$	Acknowledge	It is an input signal from a peripheral that must output low when it receives data from 8255A ports.
INTR	Interrupt Request	It is an output signal used to interrupt the MPU to request the next data byte for output.
INTE	Interrupt Enable	This is an internal flip-flop to a port and needs to be set to generate the INTR signal.

Table E3



8255 A Mode 2: Bi-directional Input/output [9]

Figure E3



8255 A Mode 2: Bi-directional Input/output [9]

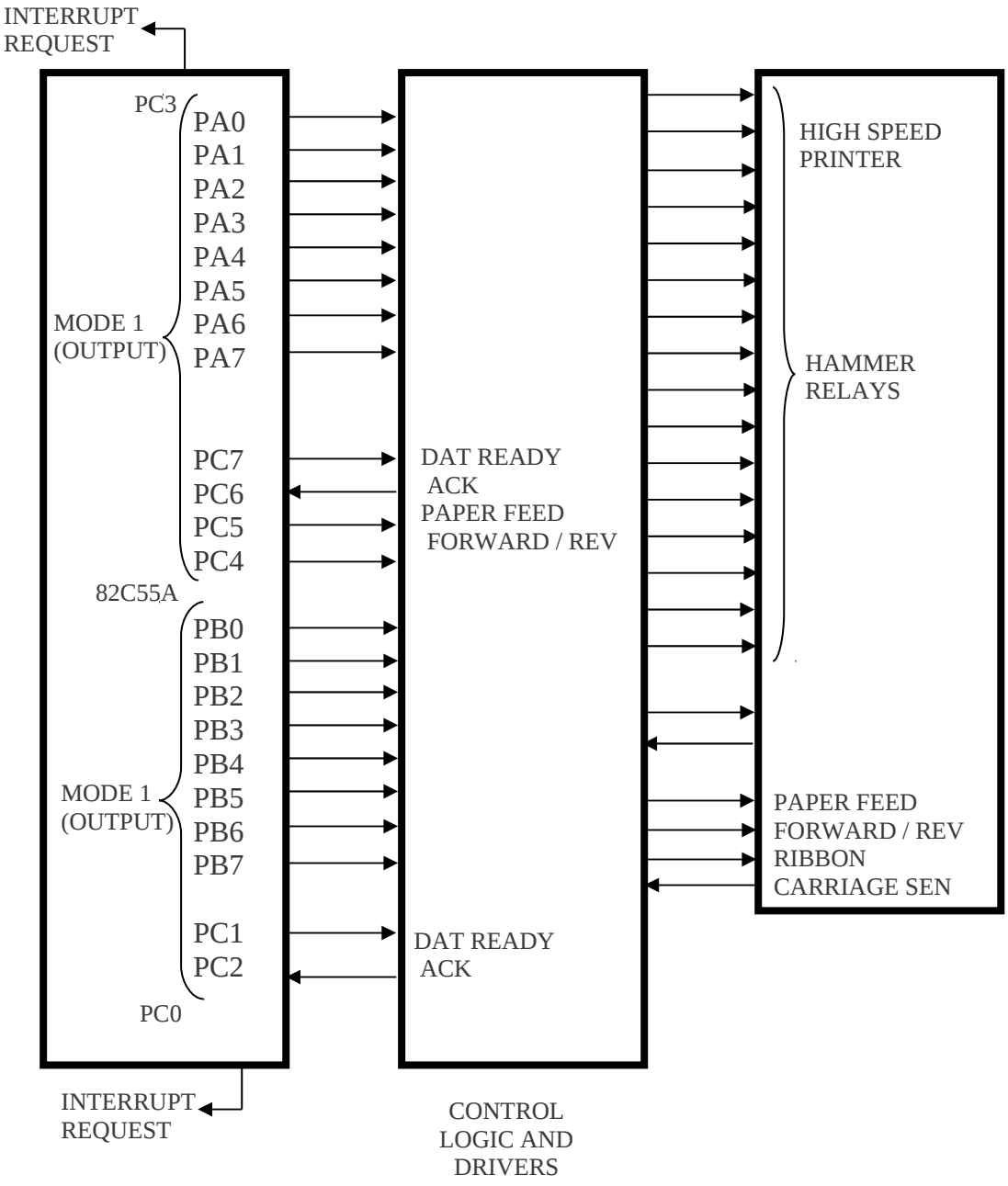
Figure E4

Bi-directional bus 1/0 control signals definition [9]

Signal	Full name	Definition
INTR	**Interrupt request**	A high on this output can be used to interrupt the CPU for both input or output operations.
$\overline{\text{OBF}}$	**Output Buffer Full**	It is an output signal that will go low to indicate that the CPU has written data out to port A.
$\overline{\text{ACK}}$	**Acknowledge**	It is used in case of the output operation. A low on this input enables the three-state output buffer of port A to send out the data. Otherwise the output buffer will be in the high impedance state.
INTE.1	**Interrupt Enable 1**	It is used in case of output operation. The INTE Flip-flop associated with $\overline{\text{OBF}}$ is controlled by bit rest of PC4.
$\overline{\text{STB}}$	**Strobe input**	It is used in case of input operation. A low on this input loads data into the input latch.
IBF	**Input Buffer Full**	It is used in case of input operation. A high on this output indicates that data has been loaded into the input latch.
INTE.2	**Interrupt Enable 2**	It is used in case of input operation. The INTE flip-flop associated with IBF and it is controlled by bit set/rest of PC4.

Table E4

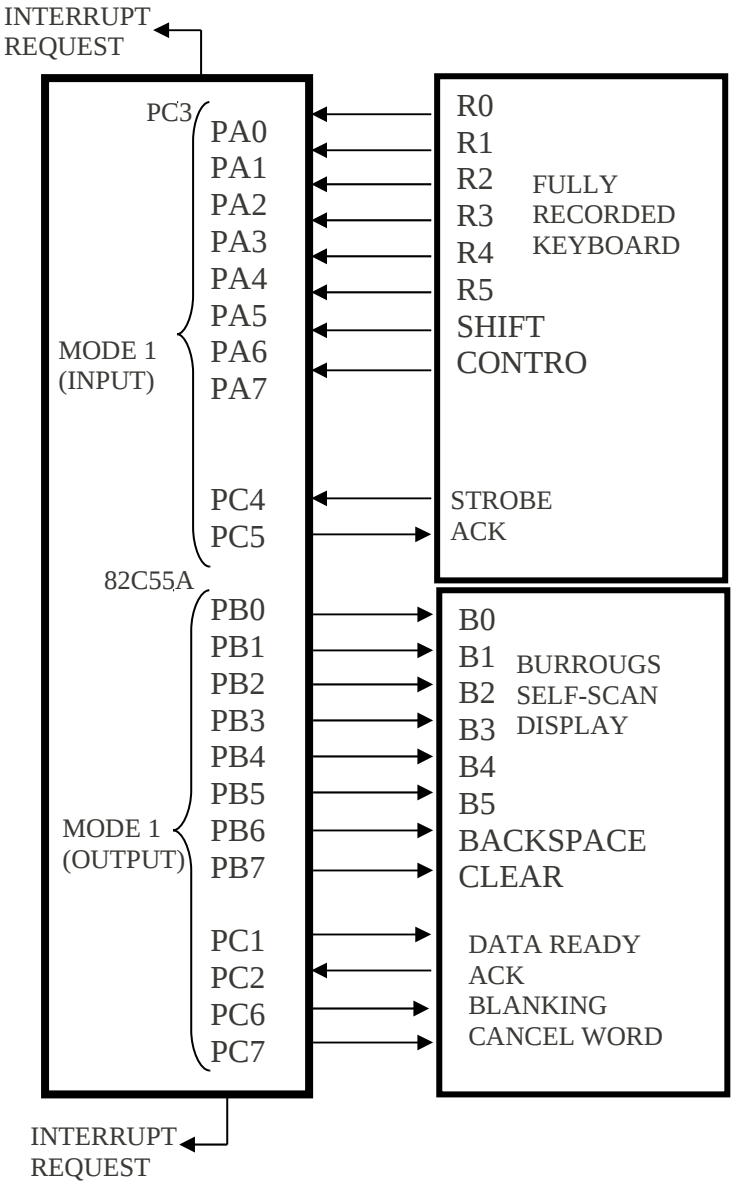
Example 1



PRINTER INTERFACE [9]

Figure F1

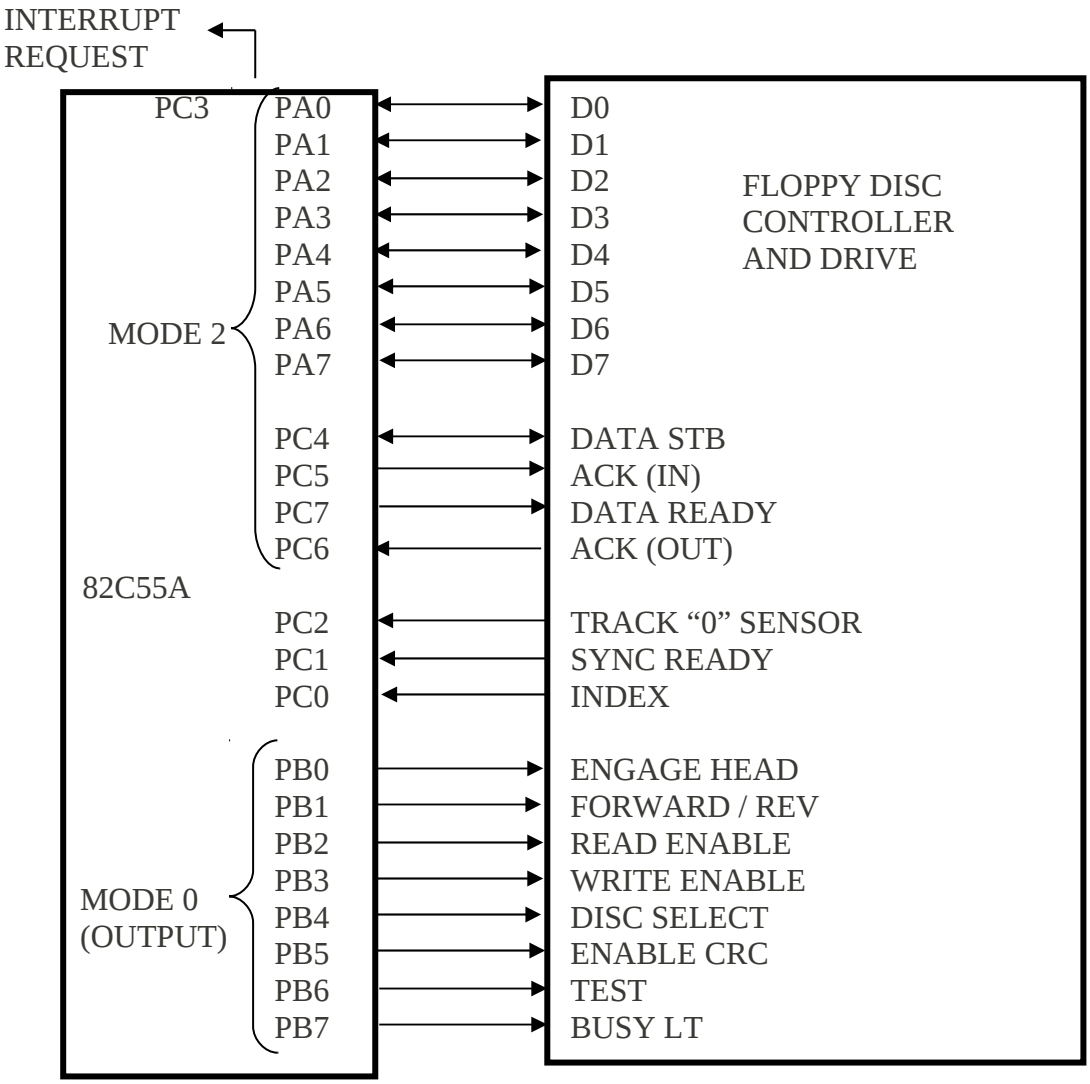
Example 2



KEYBOARD AND DISPLAY INTERFACE [9]

Figure F2

Example 3



BASIC FLOPPY DISC INTERFACE [9]

Figure F3