

List of Figures

Page No.

CHAPTER TWO TYPE OF SEQUENTIAL ELEMENTS

Figure (2.1): Clock Cycle.....	4
Figure (2.2): RS Latch.....	5
Figure (2.3): RS Latch Using NAND.....	6
Figure (2.4): RS Latch with Clock.....	7
Figure (2.5): D-Latch.....	8
Figure (2.6): JK-Latch.....	9
Figure (2.7): T-Latch.....	10
Figure (2.8): JK Master Slave.....	11

CHAPTER THREE SEQUENTIAL CONCEPT

Figure (3.1): Block Diagram of Sequential Circuit.....	12
Figure (3.2): Feed NOT gate.....	13
Figure (3.3): Output Oscillates.....	13
Figure (3.4): Cascade Two Inverters.....	14
Figure (3.5): Buffer.....	14
Figure (3.6): Inverters Connected Back to Back.....	14
Figure (3.7): RS with Active High Enable.....	15
Figure (3.8): Two Level Sensitive Memory Elements.....	16

CHAPTER FOUR HARDWARE DESIGN

Figure (4.1): Circuit Design.....	18
Figure (4.2): EPROM 2732.....	20
Figure (4.3): Connection Diagram of 74273.....	21
Figure (4.4): Logic Diagram of 74273.....	22
Figure (4.5): SN 74373.....	23
Figure (4.6): Parallel Printer Port.....	24

CHAPTER FIVE SOFTWARE

Figure (5.1): Flow Chart of Program.....	33
--	----