بِسۡمِ ٱللَّهِ ٱلرَّحۡمَٰنِ ٱلرَّحِيمِ

ٱقۡرَأۡ بِٱسۡمِ رَبِّكَ ٱلَّذِى خَلَقَ ﴿١﴾ خَلَقَ ٱلۡإِنسَٰنَ مِنۡ عَلَقٍ ﴿٢﴾

ٱقۡرَأۡ وَرَبُّكَ ٱلۡأَكۡرَمُ ﴿٣﴾ ٱلَّذِى عَلَّمَ بِٱلۡقَلَمِ ﴿٤﴾ عَلَّمَ ٱلۡإِنسَٰنَ

مَا لَمۡ يَعۡلَمۡ ﴿٥﴾

صدق الله العظيم
سورة العلق

DEDICATION

With my worm feeling, I am dedicating this thesis to the wholly great father, great mother, to my family members god bless them.

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In the name of Allah, Most Gracious, And Most Merciful Praise be Almighty Allah (Subhanahu Wa Ta'la) who gave me the courage and patience to carry out this work.

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ABSTRACT

Microprocessors are the devices in a computer that make things happen. They are capable of performing basic arithmetic operations, moving data from place to place, and making basic decisions based on the quantity of certain values. In this project a systematic step of designing of microprocessor from the ground up methodology has been described. To define the behavior of the Complex Programmable Logic Devices (CPLDs), a description of the hardware's structure and behavior was written in a High-level Hardware Description Language (VHDL) and that code was then compiled and downloaded prior to execution. The design entry step is followed or interspersed with periods of functional simulation using QuartusII software. That's where a simulator is used to execute the design and confirm that the correct outputs are produced for a given set of test inputs.

Compilation only begins after a functionally correct representation of the hardware exists. This hardware compilation consists of two distinct steps. First, an intermediate representation of the hardware design was produced. This step is called synthesis and the result of a representation called a netlist. The netlist is device independent, so its contents do not depend on the particulars of the FPGA or CPLD; it is usually stored in a standard format called the Electronic Design Interchange Format (EDIF). The second step in the translation process is called place & route. This step involves mapping the logical structures described in the netlist onto actual macrocells, interconnections, and input and output pins; this is the bitstream format.

Once the bitstream has been created a CPLD kit (ALTERA kit) was used to check the designed microprocessor performance. The generated bitstream was downloaded into max EPM7128SLC84-7.

المستخلص

المعالجات الدقيقة هى الأجهزة داخل الكمبيوتر التى ينتج عنها حدوث الأشياء.وهى قادرة على تأدية العمليات الحسابية الأساسية ، نقل البيانات من مكان لآخر واتخاذ قرارات أساسية استنادا على مجموعة من القيم المعينة. فى هذا البحث وصف لخطوة منظمة لتصميم المعالج الدقيق من اساسياته. لتعريف السلوك للأجهزة المنطقية المعقدة القابلة للبرمجة (CPLDs) فان وصف بنية المعدات الصلبة وسلوكها يكتب بلغة وصف المعدات الصلبة عالية المستوى (VHDL) وتلك الشفرة تترجم و تحمل قبل التنفيذ. الخطوة التالية عبارة عن محاكاة التصميم باستخدام برنامج Quartus II. وهنا يستخدم المحاكى لتنفيذ التصميم والتأكيد على ان المخرجات الصحيحة انتجت من مجموعة المدخلات المختبرة.

الترجمة تبدأ بعد التأكد من التمثيل الصحيح للمعدات الصلبة. تتكون ترجمة المعدات الصلبة من خطوتين: أولا اعطاء تمثيل متوسط لتصميم المعدات الصلبة وهذه الخطوة تسمى التركيب (synthesis) والنتيجة تسمى netlist . Netlist لا تعتمد على الجهاز ولذا فان مكوناته لا تعتمد علي (FPGA) أو (CPLD) معين وعادة تخزن فى صيغة قياسية تسمى صيغة تبادل التصميم الألكترونى (EDIF).

الخطوة الثانية فى عملية الترجمة تسمى place & route هذه الخطوة تشمل تخطيط للتركيب المنطقى الموصوف فى netlist لل macrocells الحقيقية، التوصيلات ومسامير الدخل والخرج وهذه هى صيغة bitstream . عندما تكون bitstream تحمل فى شريحة CPLD (ALTERA kit MAXEPM7128SLC84-7) للتأكد من أداء المعالج الدقيق المصمم.

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COMPONENTS OF MICROPROCESSORS

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MICROPROCESSOR DESIGN

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List of Abbreviations

CPU	Central Processing Unit
IC	Integrated Circuit
ALU	Arithmetic and Logic Unit
I/O	Input/Output
BCD	Binary-Coded Decimal
TI	Texas Instruments
CADC	Central Air Data Computer
DSP	Digital Signal Processors
SOC	System-On-a-Chip
GPU	Graphics Processing Units
ASIC	Application-Specific Integrated Circuits
FPGA	Field Programmable Gate Array
HDL	Hardware Description Language
CPLD	Complex Programmable Logic Devices
PLA	Programmable Logic Array
PAL	Programmable Array Logic
GAL	Generic Array Logic
FFT	Fast Fourier Transform
CLB	Configurable Logic Block
LUT	Lookup Table
SRAM	Static Random Access Memory
CRAM	Configuration Random Access Memory
VHDL	Very High Level Hardware Description Language
IEEE	Institute of Electrical and Electronics Engineers
RTL	Register Transfer Level

FA	Full Adder
LE	Logic Extender
AE	Arithmetic Extender
CE	Carry Extender
RAM	Random Access Memory
ROM	Read Only Memory
PROM	Programmable Read Only Memory
EPROM	Erasable Programmable Read Only Memory
EEPROM	Electrically Erasable Programmable Read Only Memory
MUX	Multiplexer
FSM	Finite State Machine
EC	Enoch’s Computer