Sudan University of Science and Technology
College of Graduate Studies

Direct Mapping Cache Memory Design

تصميم ذاكرة مخبأة باستخدام طريقة التخطيط المباشر

This Thesis is submitted in Fulfillment of the Requirements of the Degree of Master of Science in Electronics Engineering

Provided By:
Hajir Mohammed Awad Mustafa
Supervisor:
Dr. Abd Alrasol Jabar Alzubaidy

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DEDICATION

To my mother.

To my father.

To my brothers and sisters.

To all my friends.

To my teachers.

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Many people have earned my gratitude during the preparation of this study, some of whom are not even aware of this contribution. Thanks to all of them.

Particular appreciation to Dr.Abd alrasal Jabar Alzubaidy who has given generous helps and advises at all stages of this work.

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ABSTRACT

Today's high performance microprocessors operate at speeds that far outpace even the faster of the memory bus architectures that are commonly available. One of the biggest limitations of main memory is the wait state: period of time between operations. The most common technique used to match the speed of the memory system to that of the processor is caching.

Cache memory is the level of computer memory hierarchy situated between the processor and main memory. It is a very fast memory the processor can access much more quickly than main memory or RAM.

Cache is relatively small and expensive. It is function is to keep a copy of the data and code (instruction) currently used by the CPU. By using cache memory waiting stases are significantly reduced and the work of the processor becomes more effective.

The main idea of this search is to apply hard ware using cache memory to discuss how its increases the CPU performance. In hardware designs several components and devices are assembled to design and implement a digital circuit .This circuit is connected to a computer through a cable to transfer the data to and from computer via D-25 connector.

This hardware aided with personal computer (PC) to provide the necessary software by using C++ language which has ability to be in direct interface with computer for signaling the hardware and get result of the circuit. There is a need to interface between the circuit hardware and the CPU to manage the circuit operations, this interface is implemented through line Printer. Lastly some illustrative examples are given.

تجـــــريد

حديثا اصبحت المعالجات ذ ات الأداء العالى تعمل بسرعة تفوق اعلى سرعة نا قل ذاكرة متاح بصورة شائعة. تعتبر حالة الانتظار(الفترة الزمنية بين العمليات) من اكبر مواطن الضعف في الذاكرة الرئيسة. الت قنية الاكثر شيوعا التى تستخدم للتوافق بين سرعة نظام الذاكرة والمعاج هى الذاكرة المخبائية.

الذاكرة المخبائية هى احدى مستويات ذاكرة الحاسب الهرمية التى ت قع بين الذاكرة الرئيسة والمعالج. وهى ذاكرة تمتاز بسرعة عالية بحيث تمكن المعالج من الوصول اليها بصورة أسرع من الذاكرة الرئيسة .

الذاكرة المخبائية صغيرة الحجم نسبيا ولكنها باهظة الثمن, وظيفتها هى حفظ نسخة من البيانات والشفرات (التعليمات) المستخدمة حاليا من قبل المعالج. باستخدام الذاكرة المخبائية ت قل حالات الانتظار مما يؤدى الى زيادة كفاءة المعالج.

الفكرة الاساسية لهذه الطروحة هى تصميم دائرة الكترونية باستخدام الذاكرة المخبائية لتوضيح تأثيرها على زيادة أداء وحدة المعالجة المركزية. لتصميم الدائرة العملية جمع العديد من الاجزاء والاجهزة وتم توصيلها بالحاسب خلال نا قل بيانات D-25 لن قل البيانات من والى الحاسب.

تم تدعيم هذة الدائرة باستخدام حاسب شخصى ببرمجية بلغة C++ التى لها الم قدرة على التعامل المباشر مع الدائرة لتزويدها باشارات التحكم والبيانات واعطاء النتائج من الدائرة .هنالك حوجة للتداخل بين الدائرة ووحدة المعالجة

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List of Acronyms

RAM	Random Access Memory.
CPU	Central Processing Unit.
MHZ	Megahertz.
ROM	Read Only Memory.
SRAM	Static Random Access Memory.
DRAM	Dynamic Random Access Memory.
NUMA	Non Uniform Memory Access.
EPROM	Erasable Programmable Read Only Memory.
E EPROM	Electrically Erasable Programmable Read Only Memory.
PROM	Programmable Read Only Memory.
CD	Compact disk.
WORM	Write Once Read many.
TTL	Transistor Transistor Logic.
MIPS	Million Instruction Per Second.
BIOS	Basic Input Output System.
RISC	Reduce Instruction Set computer.
CISC	Complex Instruction Set computer.
ALU	Arithmetic Logic Unit.
PC	Program Counter.
IR	Instruction Register.
SR	Status Register.
SP	Stack Pointer.

LIFO	Last In First Out.
PAL	Programmable Array Logic.
MMU	Memory Management Unit.
FIFO	First In First Out.
CAM	Content Addressable Memory.
LFU	Least Frequently Used.
DMA	Direct Memory Access.
LPT1	Line Printer1.
LED	Light Emitting Diode.
LE	Latch Enable.
OE	Out put Enable.