

**Sudan University of Science and Technology
College of Graduate Studies**

Direct Mapping Cache Memory Design

تصميم ذاكرة مخبأة باستخدام طريقة التخطيط
المباشر

**This Thesis is submitted in Fulfillment of the
Requirements of the Degree of
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DEDICATION

To my mother.

To my father.

To my brothers and sisters.

To all my friends.

To my teachers.

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Many people have earned my gratitude during the preparation of this study, some of whom are not even aware of this contribution. Thanks to all of them.

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Finally, warm gratitude to my family and friends for their patience and understanding during the study.

ABSTRACT

Today's high performance microprocessors operate at speeds that far outpace even the faster of the memory bus architectures that are commonly available. One of the biggest limitations of main memory is the wait state: period of time between operations. The most common technique used to match the speed of the memory system to that of the processor is caching.

Cache memory is the level of computer memory hierarchy situated between the processor and main memory. It is a very fast memory the processor can access much more quickly than main memory or RAM.

Cache is relatively small and expensive. Its function is to keep a copy of the data and code (instruction) currently used by the CPU. By using cache memory waiting states are significantly reduced and the work of the processor becomes more effective.

The main idea of this search is to apply hardware using cache memory to discuss how it increases the CPU performance. In hardware designs several components and devices are assembled to design and implement a digital circuit. This circuit is connected to a computer through a cable to transfer the data to and from computer via D-25 connector.

This hardware aided with personal computer (PC) to provide the necessary software by using C++ language which has ability to be in direct interface with computer for signaling the hardware and get result of the circuit. There is a need to interface between the circuit hardware and the CPU to manage the circuit operations, this interface is implemented through line Printer. Lastly some illustrative examples are given.

تجريد

حديثاً أصبحت المعالجات ذات الأداء العالي تعمل بسرعة تفوق أعلى سرعة نقل ذاكرة متاح بصورة شائعة. تعتبر حالة الانتظار (الفترة الزمنية بين العمليات) من أكبر مواطن الضعف في الذاكرة الرئيسية. التقنية الأكثر شيوعاً التي تستخدم للتواافق بين سرعة نظام الذاكرة والمعالج هي الذاكرة المخابية.

الذاكرة المخابية هي أحدى مستويات ذاكرة الحاسوب الهرمية التي تقع بين الذاكرة الرئيسية والمعالج. وهي ذاكرة تمتاز بسرعة عالية بحيث تمكن المعالج من الوصول إليها بصورة أسرع من الذاكرة الرئيسية.

الذاكرة المخابية صغيرة الحجم نسبياً ولكنها باهظة الثمن، وظيفتها هي حفظ نسخة من البيانات والشفرات (التعليمات) المستخدمة حالياً من قبل المعالج. باستخدام الذاكرة المخابية تقل حالات الانتظار مما يؤدي إلى زيادة كفاءة المعالج.

الفكرة الأساسية لهذه الطروحة هي تصميم دائرة الكترونية باستخدام الذاكرة المخابية لتوضيح تأثيرها على زيادة أداء وحدة المعالجة المركزية. لتصميم الدائرة العملية جمع العديد من الأجزاء والاجهزه وتم توصيلها بالحاسوب خلال نقل بيانات D-25 لذلقي البيانات من والى الحاسوب.

تم تدعيم هذه الدائرة باستخدام حاسب شخصي ببرمجة بلغة C++ التي لها المقدرة على التعامل المباشر مع الدائرة لتزويدها باشارات التحكم والبيانات واعطاء النتائج من الدائرة. هناك حوجة للتدخل بين الدائرة ووحدة المعالجة

المركزية لادارة عمليات الدائرة هذا التداخل تم باستخدام منفذ الطابعة .أخيرا تم
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List of Acronyms

RAM	Random Access Memory.
CPU	Central Processing Unit.
MHZ	Megahertz.
ROM	Read Only Memory.
SRAM	Static Random Access Memory.
DRAM	Dynamic Random Access Memory.
NUMA	Non Uniform Memory Access.
EPROM	Erasable Programmable Read Only Memory.
E EPROM	Electrically Erasable Programmable Read Only Memory.
PROM	Programmable Read Only Memory.
CD	Compact disk.
WORM	Write Once Read many.
TTL	Transistor Transistor Logic.
MIPS	Million Instruction Per Second.
BIOS	Basic Input Output System.
RISC	Reduce Instruction Set computer.
CISC	Complex Instruction Set computer.
ALU	Arithmetic Logic Unit.
PC	Program Counter.
IR	Instruction Register.
SR	Status Register.
SP	Stack Pointer.

LIFO	Last In First Out.
PAL	Programmable Array Logic.
MMU	Memory Management Unit.
FIFO	First In First Out.
CAM	Content Addressable Memory.
LFU	Least Frequently Used.
DMA	Direct Memory Access.
LPT1	Line Printer1.
LED	Light Emitting Diode.
LE	Latch Enable.
OE	Out put Enable.