

SN74LS373, SN74LS374

Octal Transparent Latch with 3-State Outputs; Octal D-Type Flip-Flop with 3-State Output

The SN74LS373 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data (data changes asynchronously) when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH the bus output is in the high impedance state.

The SN74LS374 is a high-speed, low-power Octal D-type Flip-Flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A buffered Clock (CP) and Output Enable (OE) is common to all flip-flops. The SN74LS374 is manufactured using advanced Low Power Schottky technology and is compatible with all ON Semiconductor TTL families.

- Eight Latches in a Single Package
- 3-State Outputs for Bus Interfacing
- Hysteresis on Latch Enable
- Edge-Triggered D-Type Inputs
- Buffered Positive Edge-Triggered Clock
- Hysteresis on Clock Input to Improve Noise Margin
- Input Clamp Diodes Limit High Speed Termination Effects

GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	4.75	5.0	5.25	V
T _A	Operating Ambient Temperature Range	0	25	70	°C
I _{OH}	Output Current – High			-2.6	mA
I _{OL}	Output Current – Low			24	mA



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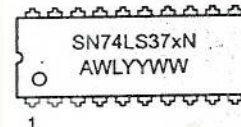
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**LOW
POWER
SCHOTTKY**

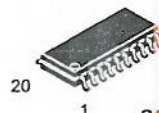
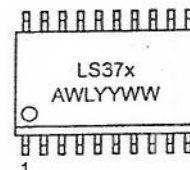
MARKING DIAGRAMS



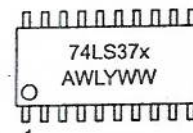
PDIP-20
N SUFFIX
CASE 738



SOIC-20
DW SUFFIX
CASE 751D



SOEIAJ-20
M SUFFIX
CASE 967



x = 3 or 4
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

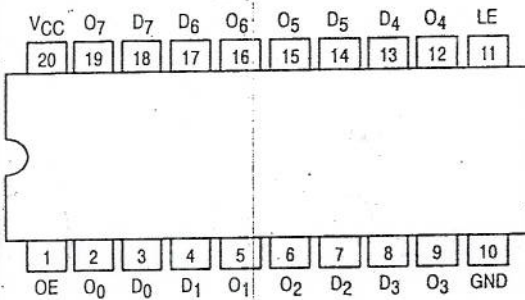
ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

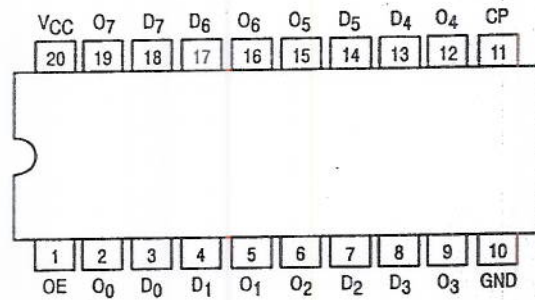
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CONNECTION DIAGRAM DIP (TOP VIEW)

SN74LS373



SN74LS374



NOTE:
The Flatpak version
has the same pinouts
(Connection Diagram) as
the Dual In-Line Package.

PIN NAMES

D₀ - D₇ Data Inputs
LE Latch Enable (Active HIGH) Input
CP Clock (Active HIGH Going Edge) Input
OE Output Enable (Active LOW) Input
O₀ - O₇ Outputs

NOTES:

a) 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.

LOADING (Note a)

HIGH	LOW
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
65 U.L.	15 U.L.

TRUTH TABLE

LS373

D _n	LE	OE	O _n
H	H	L	H
L	H	L	L
X	L	L	Q ₀
X	X	H	Z*

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

* Note: Contents of flip-flops unaffected by the state of the Output Enable input (OE).

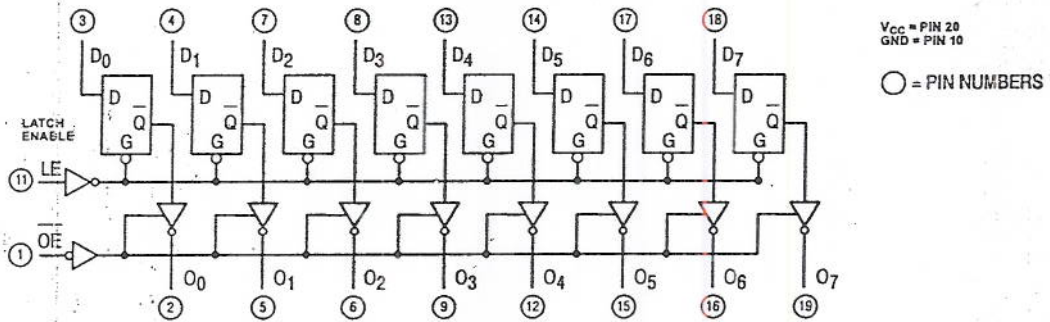
LS374

D _n	LE	OE	O _n
H		L	H
L		L	L
X	X	H	Z*

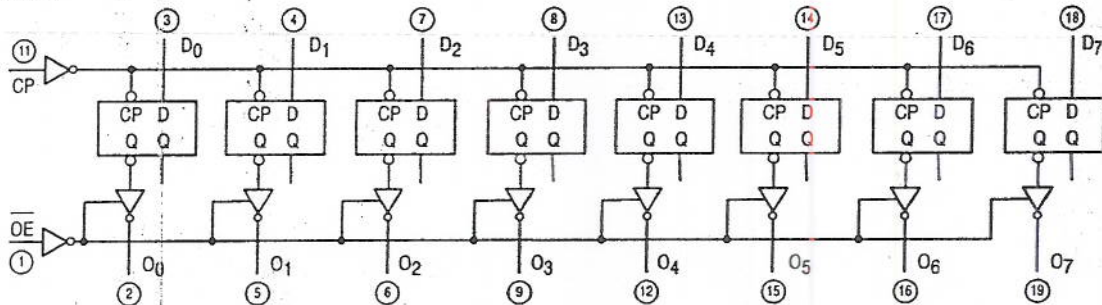
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LOGIC DIAGRAMS

SN74LS373



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DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	2.4	3.1		V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table
V _{OL}	Output LOW Voltage		0.25	0.4	V	I _{OL} = 12 mA
			0.35	0.5	V	I _{OL} = 24 mA
I _{OZH}	Output Off Current HIGH			20	μA	V _{CC} = MAX, V _{OUT} = 2.7 V
I _{OZL}	Output Off Current LOW			-20	μA	V _{CC} = MAX, V _{OUT} = 0.4 V
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V
I _{OS}	Short Circuit Current (Note 1)	-30		-130	mA	V _{CC} = MAX
I _{CC}	Power Supply Current			40	mA	V _{CC} = MAX

1. Not more than one output should be shorted at a time, nor for more than 1 second.

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AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$)

AC CHARACTERISTICS (T _A = 25°C, V _{CC} = 5.0 V)									
Symbol	Parameter	Limits						Unit	Test Conditions
		LS373			LS374				
		Min	Typ	Max	Min	Typ	Max		
f _{MAX}	Maximum Clock Frequency				35	50		MHz	C _L = 45 pF, R _L = 667 Ω
t _{PLH} t _{PHL}	Propagation Delay, Data to Output		12 12	18 18				ns	
t _{PLH} t _{PHL}	Clock or Enable to Output		20 18	30 30		15 19	28 28	ns	
t _{PZH} t _{PZL}	Output Enable Time		15 25	28 36		20 21	28 28	ns	
t _{PHZ} t _{PLZ}	Output Disable Time		12 15	20 25		12 15	20 25	ns	C _L = 5.0 pF

AC SETUP REQUIREMENTS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$)

AC SETUP REQUIREMENTS (T _A = 25°C, V _{CC} = 5.0 V)						
Symbol	Parameter	Limits				Unit
		LS373		LS374		
		Min	Max	Min	Max	
t _W	Clock Pulse Width	15		15		ns
t _s	Setup Time	5.0		20		ns
t _h	Hold Time	20		0		ns

DEFINITION OF TERMS

SETUP TIME (t_S) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to LE transition from HIGH-to-LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_H) — is defined as the minimum time following the LE transition from HIGH-to-LOW that the logic level must be maintained at the input in order to ensure continued recognition.

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AC WAVEFORMS

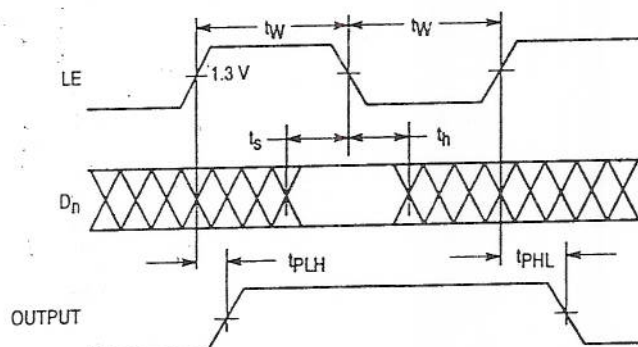


Figure 1.

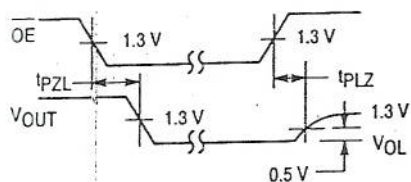


Figure 2.

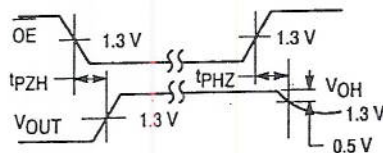
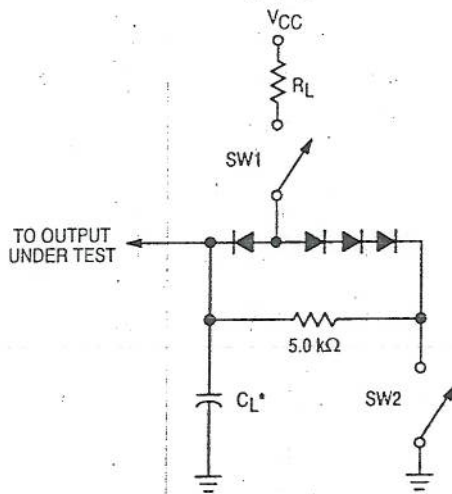


Figure 3.

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SN74LS373

AC LOAD CIRCUIT



* Includes Jig and Probe Capacitance.

Figure 4.

SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

SN74LS374

AC WAVEFORMS

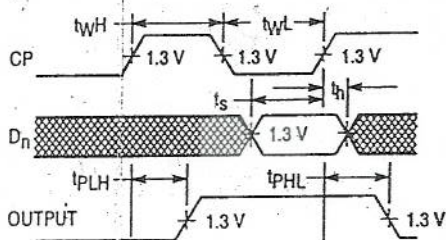


Figure 5.

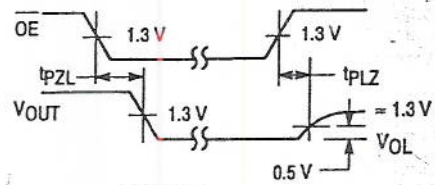


Figure 6.

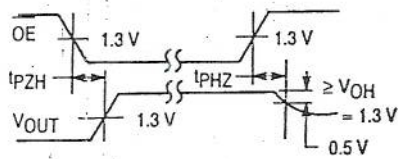
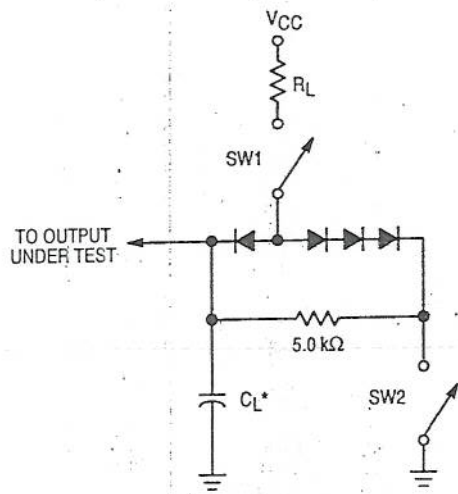


Figure 7.

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SN74LS374

AC LOAD CIRCUIT



* Includes Jig and Probe Capacitance.

SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

Figure 8.

DEVICE ORDERING INFORMATION

Device Order Number	Package Type	Tape and Reel Size
SN74LS373N	PDIP-20	1440 Units/Box
SN74LS373DW	SOIC-WIDE	38 Units/Rail
SN74LS373DWR2	SOIC-WIDE	2500/Tape and Reel
SN74LS373M	SOEIAJ-20	See Note 2
SN74LS373MEL	SOEIAJ-20	See Note 2
SN74LS374N	PDIP-20	1440 Units/Box
SN74LS374DW	SOIC-WIDE	38 Units/Rail
SN74LS374DWR2	SOIC-WIDE	2500/Tape and Reel
SN74LS374M	SOEIAJ-20	See Note 2
SN74LS374MEL	SOEIAJ-20	See Note 2

2. For ordering information on the EIAJ version of the SOIC package, please contact your local ON Semiconductor representative.

PACKAGE DIMENSIONS

Technical drawing of a 20-pin D-sub connector. The drawing includes three views: a top view, a side view, and a detail view of the contact pins.

Top View: Shows the 20-pin connector with dimensions A (overall width) and B (height). Pin numbers 1, 10, 11, and 20 are indicated.

Side View: Shows the connector's profile with dimensions C (height to top of housing), K (height to top of contact pins), and N (height to bottom of contact pins). The **SEATING PLANE** is indicated.

Detail View: Shows the contact pins with dimensions E (pin length), F (pin diameter), G (pin spacing), and D (pin diameter at base). The base is labeled **D 20 PL**.

Dimensional Table:

$\oplus$	0.25 (0.010)	(M)	T	A	(M)
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Feature Callouts:

- T-** SEATING PLANE
- A-** Overall width
- B** Height
- C** Height to top of housing
- K** Height to top of contact pins
- N** Height to bottom of contact pins
- E** Pin length
- F** Pin diameter
- G** Pin spacing
- D 20 PL** Pin diameter at base
- L** Housing length
- M** Housing thickness
- J 20 PL** Housing diameter at base

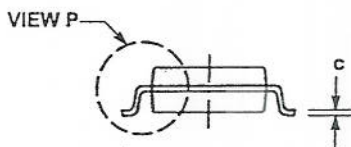
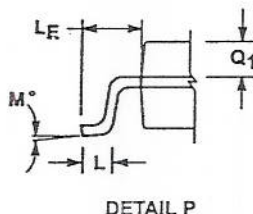
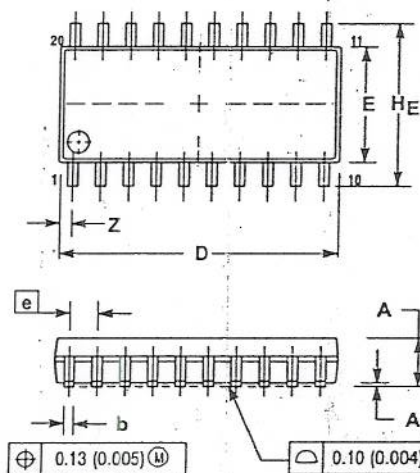
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.10	1.70	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
ø	0°	7°

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PACKAGE DIMENSIONS

M SUFFIX
SOEIAJ PACKAGE
CASE 967-01
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.005) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	2.05	—	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	12.35	12.80	0.486	0.504
E	5.10	5.45	0.201	0.215
e	1.27 BSC	—	0.050 BSC	—
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q ₁	0.70	0.90	0.028	0.035
Z	—	0.81	—	0.032

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