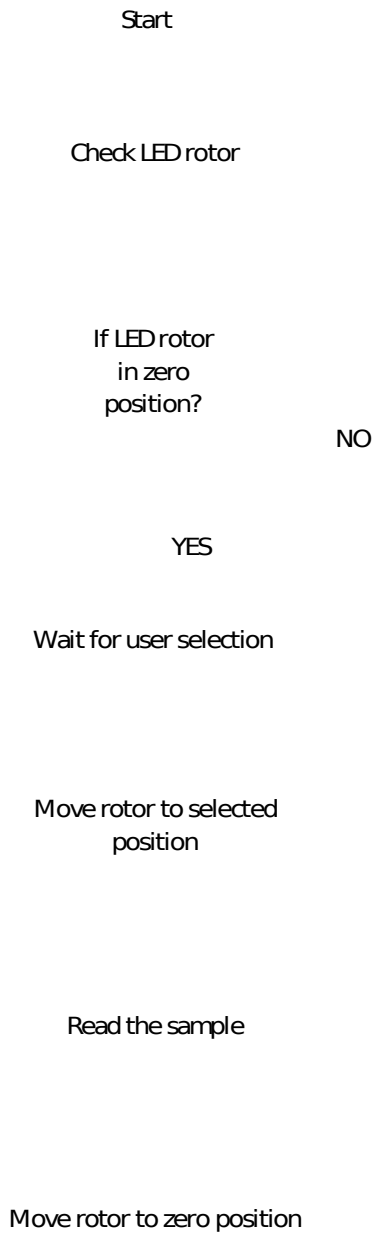


APPENDIX A flow chart of program



APPENDIX B

spectrophotometer control program using basic language:

```
$regfile = "m32def.dat"  
$crystal = 8000000
```

```
Config Lcd = 16 * 2  
Config Lcdpin = Pin , Db4 =  
Portb.4 , Db5 = Portb.5 , Db6 =
```

Portb.6 , Db7 = Portb.7 , Rs =
Portb.0 , E = Portb.1
Config Porta.0 = Output
Config Porta.1 = Output
Config Porta.2 = Output
Config Porta.3 = Output
Config Porta.4 = Input
Config Pina.5 = Input
Config Pina.6 = Input
Config Pina.7 = Input
Config Pind.0 = Input
Config Pind.1 = Input
Config Pind.2 = Input
Config Pind.3 = Input
Config Portd.4 = Output
Config Portc = Input

Dim D As Byte , I As Byte

Cursor Off:
Cls

Lcd "TESTING MODE."

Cursor Off:
Cls
Locate 1 , 1
Lcd "TO SELECT UV"
Locate 2 , 1
Lcd "FILTER PRESS SW1"
Waitms 200
Locate 1 , 1
Cls
Locate 1 , 1
Lcd "TO SELECT RED"
Locate 2 , 1
Lcd "FILTER PRESS SW2"
Waitms 200
Locate 1 , 1
Cls

Locate 1 , 1
Lcd "TO SELECT GREEN"
Locate 2 , 1
Lcd "FILTER PRESS SW3"
Waitms 200
Locate 1 , 1
Locate 1 , 1
Lcd "TO SELECT YELLOW"
Locate 2 , 1
Lcd "FILTER PRESS SW4"
Waitms 200
Locate 1 , 1
Cls
Locate 1 , 1
Lcd "TO SELECT BLUE"
Locate 2 , 1
Lcd "FILTER PRESS SW5"
Waitms 200
Locate 1 , 1
Lcd "error position"

While Pind.3 = 1

Porta.0 = 1
Waitms 100
Porta.0 = 0
Porta.1 = 1
Waitms 100
Porta.1 = 0
Porta.2 = 1
Waitms 100
Porta.2 = 0
Porta.3 = 1
Waitms 100
Porta.3 = 0
Wend

Do

Locate 1 , 1
Lcd "WELCOME"

```

If Pina.4 = 0 Then

Cls
Locate 1 , 1
Lcd "running motor"
For I = 1 To 2
Porta.0 = 1
Waitms 100
Porta.0 = 0
Porta.1 = 1
Waitms 100
Porta.1 = 0
Porta.2 = 1
Waitms 100
Porta.2 = 0
Porta.3 = 1
Waitms 100
Porta.3 = 0
Next
Cls
Lcd "UV filter"
Portd.4 = 1
Waitms 3000
Portd.4 = 0

Cls
Lcd "finish UV"
Locate 2 , 1
Lcd "test"
Waitms 200
Cls
End If

```

' Select RED filter

```

If Pina.5 = 0 Then

Cls
Locate 1 , 1
Lcd "running motor"
For I = 1 To 4

Porta.0 = 1
Waitms 100
Porta.0 = 0
Porta.1 = 1
Waitms 100
Porta.1 = 0
Porta.2 = 1
Waitms 100
Porta.2 = 0
Porta.3 = 1
Waitms 100
Porta.3 = 0
Waitms 50
Porta.3 = 0
Next
Cls
Lcd "RED filter"
Portd.4 = 1
Waitms 3000
Portd.4 = 0

Cls
Lcd "finish RED"
Locate 2 , 1
Lcd "test"
Waitms 200
Cls
End If

```

' Select GREEN filter

If Pina.6 = 0 Then

```
Cls
Locate 1 , 1
Lcd "running motor"
```

```
For I = 1 To 6
```

```
Porta.0 = 1
Waitms 100
Porta.0 = 0
Porta.1 = 1
Waitms 100
Porta.1 = 0
Porta.2 = 1
Waitms 100
Porta.2 = 0
Porta.3 = 1
Waitms 100
Porta.3 = 0
```

```
Next
```

```
Cls
Lcd "GREEN filter"
Portd.4 = 1
Waitms 3000
Portd.4 = 0
```

```
Cls
Locate 1 , 1
Lcd "finish GREEN"
Locate 2 , 1
Lcd "test"
Waitms 200
Cls
```

```
End If
```

```
' Select YELLOW filter
```

If Pina.7 = 0 Then

```
Cls
Lcd "running motor"
For I = 1 To 8
Locate 1 , 1
Porta.0 = 1
Waitms 100
Porta.0 = 0
Porta.1 = 1
Waitms 100
Porta.1 = 0
Porta.2 = 1
Waitms 100
Porta.2 = 0
Porta.3 = 1
Waitms 100
Porta.3 = 0
Next
Cls
Lcd "YELLOW filter"
Portd.4 = 1
Waitms 3000
Portd.4 = 0
```

```
Cls
Lcd "finish YELLOW"
Locate 2 , 1
Lcd "test"
Waitms 200
Cls

End If
```

```
' Select BLUE filter
```

```

If Pinc.0 = 0 Then

Cls
Locate 1 , 1
Lcd "running motor"

For I = 1 To 10
Porta.0 = 1
Waitms 100
Porta.0 = 0
Porta.1 = 1
Waitms 100
Porta.1 = 0
Porta.2 = 1
Waitms 100
Porta.2 = 0
Porta.3 = 1
Waitms 100
Porta.3 = 0
Next
Cls
Lcd "BLUE filter"
Portd.4 = 1
Waitms 3000
Portd.4 = 0

Cls
Lcd "finish BLUE"
Locate 2 , 1
Lcd "test"
Waitms 200
Cls
End If

Loop
End

```

APPENDIX C ADC and USART program using basic language:

```

$regfile = "m32def.dat"

$crystal = 8000000

$baud = 19200

Config Adc = Single ,
Prescaler = Auto

Start Adc

Const X = 1000

Dim Y As Single
Dim Z As Single
Dim M As Single
Dim S As Single
Dim R As Single
Dim A As Word
Dim B As Word
Dim C As Word
Dim D As Word

While D =1

Do

A = Getadc(0)

Y = A

Y = Y / 0.01

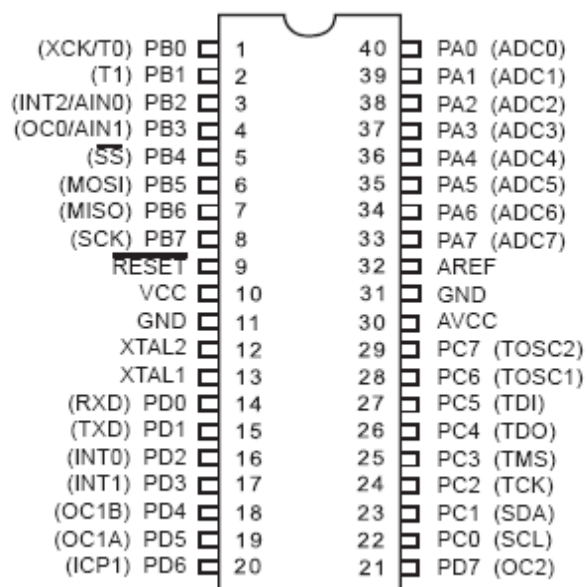
```

```

Y = Y * X
Print "READING OF M = M / 0.01
BLANK:" ;
M = M * X
Waitms 1000
Print "READING OF
B = Getadc(0)
SAMPLE:" ; M
Z = B
Waitms 1000
Z = Z / 0.01
S = M / Z
Z = Z * X
Print "FINAL RESULT = " ; S
Print "READING OF Waitms 1000
STANDARD:" ; Z
Loop
Waitms 1000
EndLoop
C = Getadc(0)
End

```

APPENDIX D Atmega32 &16 datasheet:



Pin out atmega32.

Features

- High-performance, Low-power AVR® 8-bit Microcontroller
- Advanced RISC Architecture
 - 131 Powerful Instructions – Most Single-clock Cycle Execution
 - 32 × 8 General Purpose Working Registers
 - Fully Static Operation
 - Up to 16 MIPS Throughput at 16 MHz
 - On-chip 2-cycle Multiplier
- High Endurance Non-volatile Memory segments
 - 32 Kbytes of In-System Self-programmable Flash program memory
 - 1024 Bytes EEPROM
 - 2 Kbytes Internal SRAM
 - Write/Erase Cycles: 10,000 Flash/100,000 EEPROM
 - Data retention: 20 years at 85°C/100 years at 25°C
 - Optional Boot Code Section with Independent Lock Bits

In-System Programming by On-chip Boot Program

True Read-While-Write Operation

- Programming Lock for Software Security
- JTAG (IEEE std. 1149.1 Compliant) Interface
 - Boundary-scan Capabilities According to the JTAG Standard
 - Extensive On-chip Debug Support

– Programming of Flash, EEPROM, Fuses, and Lock Bits through the JTAG Interface

- Peripheral Features

- Two 8-bit Timer/Counters with Separate Prescalers and Compare Modes

- One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and

Capture

Mode

- Real Time Counter with Separate Oscillator

- Four PWM Channels

- 8-channel, 10-bit ADC

8 Single-ended Channels

7 Differential Channels in TQFP Package Only

2 Differential Channels with Programmable Gain at 1x, 10x, or 200x

- Byte-oriented Two-wire Serial Interface

- Programmable Serial USART

- Master/Slave SPI Serial Interface

- Programmable Watchdog Timer with Separate On-chip Oscillator

- On-chip Analog Comparator

- Special Microcontroller Features

- Power-on Reset and Programmable Brown-out Detection

- Internal Calibrated RC Oscillator

- External and Internal Interrupt Sources

– Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby

and Extended Standby

- I/O and Packages

- 32 Programmable I/O Lines

- 40-pin PDIP, 44-lead TQFP, and 44-pad QFN/MLF

- Operating Voltages

- 2.7V - 5.5V for ATmega32L

- 4.5V - 5.5V for ATmega32

- Speed Grades

- 0 - 8 MHz for ATmega32L

- 0 - 16 MHz for ATmega32

- Power Consumption at 1 MHz, 3V, 25°C for ATmega32L

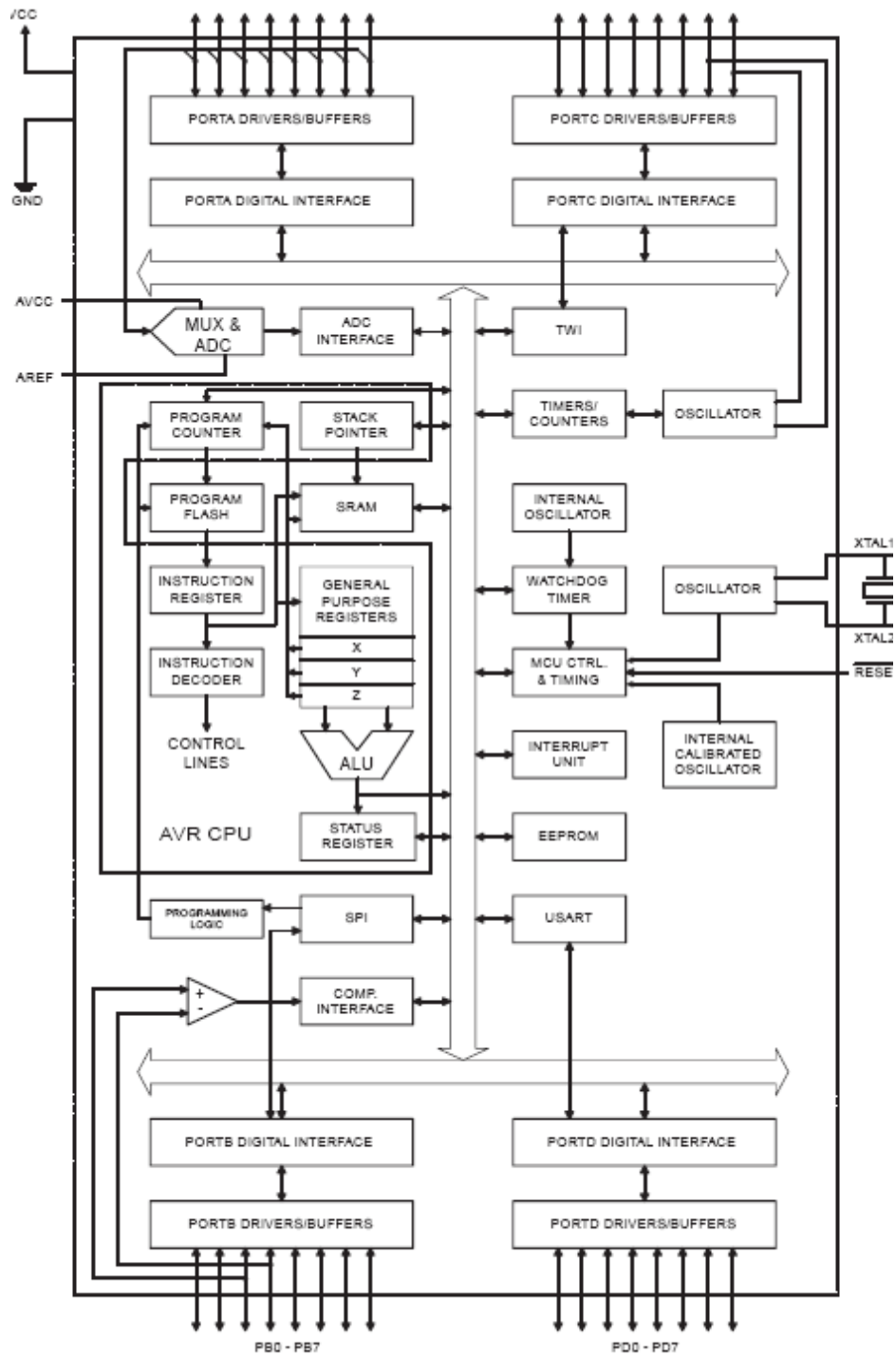
- Active: 1.1 mA

- Idle Mode: 0.35 mA

- Power-down Mode: < 1 μ A

Overview

The ATmega32 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega32 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.



Atmega32 block diagram.

The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic

Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATmega32 provides the following features: 32 Kbytes of In-System Programmable Flash Program memory with Read-While-Write capabilities, 1024 bytes EEPROM, 2K byte SRAM, 32 general purpose I/O lines, 32 general purpose working registers, a JTAG interface for Boundary scan, On-chip Debugging support and programming, three flexible Timer/Counters with compare modes, Internal and External Interrupts, a serial programmable USART, a byte oriented Two-wire Serial Interface, an 8-channel, 10-bit ADC with optional differential input stage with programmable gain (TQFP package only), a programmable Watchdog Timer with Internal Oscillator, an SPI serial port, and six software selectable power saving modes. The Idle mode stops the CPU while allowing the USART, Two-wire interface, A/D Converter, SRAM; Timer/Counters, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next External Interrupt or Hardware Reset. In Power-save mode, the Asynchronous Timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except Asynchronous Timer and ADC, to minimize switching noise during ADC conversions. In Standby mode, the crystal/resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low-power consumption. In Extended Standby mode, both the main Oscillator and the Asynchronous Timer continue to run. The device is manufactured using Atmel's high density nonvolatile memory technology. The On chip ISP Flash allows the program memory to be reprogrammed in-system through

an SPI serial interface, by a conventional nonvolatile memory programmer, or by an On-chip Boot program running on the AVR core. The boot program can use any interface to download the application program in the Application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATmega32 is a powerful microcontroller that provides a highly-flexible and cost-effective solution to many embedded control applications.

The ATmega32 AVR is supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, in-circuit emulators, and evaluation kits.

Pin Descriptions

VCC: Digital supply voltage.

GND: Ground.

Port A (PA7...PA0) Port A serves as the analog inputs to the A/D Converter.

Port A also serves as an 8-bit bi-directional I/O port, if the A/D Converter is not used. Port pins can provide internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability. When pins PA0 to PA7 are used as inputs and are externally pulled low, they will source current if the internal pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B (PB7...PB0) Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up

resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running. Port B also serves the functions of various special features of the ATmega32.

Port C (PC7...PC0) Port C is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running. If the JTAG interface is enabled, the pull-up resistors on pins PC5 (TDI), PC3 (TMS) and PC2 (TCK) will be activated even if a reset occurs. The TD0 pin is tri-stated unless TAP states that shift out data are entered. Port C also serves the functions of the JTAG interface and other special features of the ATmega32.

Port D (PD7...PD0) Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running. Port D also serves the functions of various special features of the ATmega32.

RESET: Reset Input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. Shorter pulses are not guaranteed to generate a reset.

XTAL1: Input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

XTAL2: Output from the inverting Oscillator amplifier.

AVCC: AVCC is the supply voltage pin for Port A and the A/D Converter. It should be externally connected to VCC, even if the ADC is not used. If the ADC is used, it should be connected to VCC through a low-pass filter.

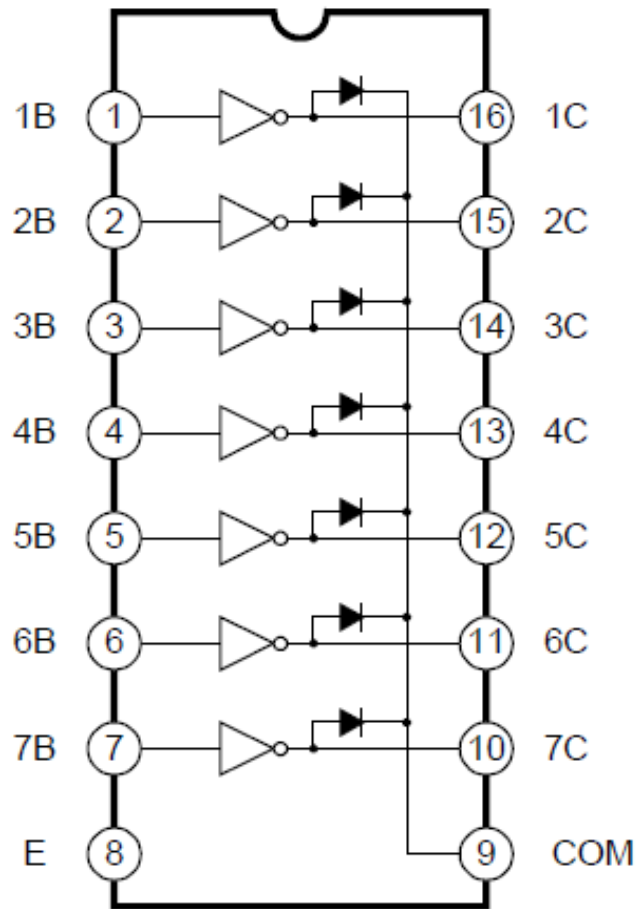
AREF: AREF is the analog reference pin for the A/D Converter.

ULN2003 datasheet:

DESCRIPTION:

The ULN2001A, ULN2002A, ULN2003 and ULN2004A are high voltage, high current Darlington arrays each containing seven open collector Darlington pairs with common emitters. Each channel rated at 500mA and can withstand peak currents of 600mA. Suppression diodes are included for inductive load driving and the inputs are pinned opposite outputs to simplify board layout. The four versions interface to all common logic families: These versatile devices are useful for driving a wide loads including solenoids, relays DC motors, LED displays filament lamps, thermal print heads and high power buffers. The ULN2001A/2002A/2003A and 2004A are supplied in 16 pin plastic DIP packages with a copper lead frame to reduce thermal resistance.

LOGIC DIAGRAM



Pin connection of ULN2003.

APPENDIX E USART interface code using MATLAB:

```
% Set serial port mode

!mode com3:9600, n, 8, 1

% open com port for data transfer

fid = fopen('com3:', 'w');

fwrite(fid, 'data', 'int8');

% send reset pulse

fwrite(fid, 255, 'int8');

% close com port connection

fclose(fid);
```

APPENDIX F unipolar motor datasheet:

PM35L_048 datasheet:

- Motor Size: PM35L-048.
- Number of Steps per Rotation 48(7.5°/Step).
- Drive Method: 2-2 PHASE.
- Drive Circuit: UNIPOLAR CONST. VOLT.
- Drive Voltage: 24[V].
- Current/Phase: 500[mA].
- Coil Resistance/Phase: 30[Ω].
- Drive IC: 2SC3346.
- Magnet Material: Ferrite plastic magnet (MSPL) Polar anisotropy ferrite sintered magnet (MS50) Nd-Fe-B bonded magnet (MS70).
- Insulation Resistance: 100M[Ω] MIN.
- Dielectric Strength: AC 500[V] 1[min].
- Class of Insulation: CLASS E.
- Operating Temp: -10[°C] ~ 50[°C].
- Storage Temp. -30[°C] ~ 80[°C].
- Operating Hum. 20[%] RH ~ 90[%] RH.

Applications:

- OA Equipment: Printers / Scanners.
- Automotive: Meters / Optic axis control device.
- Industrial equipment: Flow control valves.
- Home automation appliances: Sewing machines.

APPENDIX G temperature sensor:

BPX 65 datasheet:

Features:

- Especially suitable for applications from 350 nm to 1100 nm.
- BPX 65: high photosensitivity.
- Hermetically sealed metal package (TO-18), suitable up to 125 C⁰.

Applications:

- Fast optical sensor of high modulation bandwidth.

18 A3 DIN 41870, flat glass lens, hermetically sealed package, solder tabs 2.54 mm (2/10”) lead spacing, anode marking: projection at package bottom.

- Operating and storage temperature range (T_{stg}): $-40 \dots +125 \text{ C}^0$.
- Soldering temperature in 2 mm distance from case bottom ($t \leq 3 \text{ ms}$) (TS): 230 C^0 .
- Reverse voltage (V_R): 50 V.
- Total power dissipation (P_{tot}): 250 mW.

APPENDIX H Max232 datasheet:

- Meet or Exceed TIA/EIA-232-F and ITU Recommendation V.28
- Operate With Single 5-V Power Supply
- Operate Up to 120 kbit/s
- Two Drivers and Two Receivers
- ± 30 -V Input Levels
- Low Supply Current . . . 8 mA Typical
- Designed to be Interchangeable With Maxim MAX232
- ESD Protection Exceeds JESD 22 – 2000-V Human-Body Model (A114-A)
- Applications

TIA/EIA-232-F

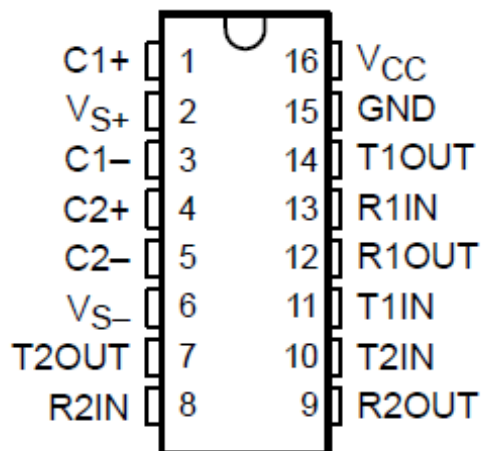
Battery-Powered Systems

Terminals

Modems

Computers

Description/ordering information:



The MAX232 is a dual driver/receiver that includes a capacitive voltage generator to supply EIA-232 voltage levels from a single 5-V supply. Each receiver converts EIA-232 inputs to 5-V TTL/CMOS levels. These receivers have a typical threshold of 1.3 V and a typical hysteresis of 0.5 V, and can accept ± 30 -V inputs. Each driver converts TTL/CMOS input levels into EIA-232 levels. The driver, receiver, and voltage-generator functions are available as cells in the Texas Instruments LinASIC™ library.

ORDERING INFORMATION

T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP (N)	Tube	MAX232N	MAX232N
	SOIC (D)	Tube	MAX232D	MAX232
		Tape and reel	MAX232DR	
	SOIC (DW)	Tube	MAX232DW	MAX232
		Tape and reel	MAX232DWR	
SOP (NS)	Tape and reel	MAX232NSR	MAX232	
-40°C to 85°C	PDIP (N)	Tube	MAX232IN	MAX232IN
	SOIC (D)	Tube	MAX232ID	MAX232I
		Tape and reel	MAX232IDR	
	SOIC (DW)	Tube	MAX232IDW	MAX232I
		Tape and reel	MAX232IDWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Function Tables

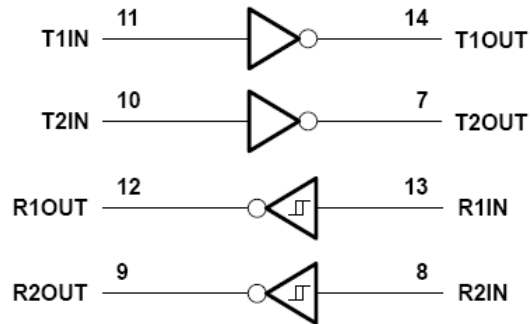
EACH DRIVER	
INPUT T _{IN}	OUTPUT T _{OUT}
L	H
H	L

H = high level, L = low level

EACH RECEIVER	
INPUT R _{IN}	OUTPUT R _{OUT}
L	H
H	L

H = high level, L = low level

logic diagram (positive logic)



Absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input supply voltage range, V _{CC} (see Note 1)	-0.3 V to 6 V
Positive output supply voltage range, V _{S+}	V _{CC} - 0.3 V to 15 V
Negative output supply voltage range, V _{S-}	-0.3 V to -15 V
Input voltage range, V _I : Driver	-0.3 V to V _{CC} + 0.3 V
Receiver	±30 V
Output voltage range, V _O : T1OUT, T2OUT	V _{S-} - 0.3 V to V _{S+} + 0.3 V
R1OUT, R2OUT	-0.3 V to V _{CC} + 0.3 V
Short-circuit duration: T1OUT, T2OUT	Unlimited
Package thermal impedance, θ _{JA} (see Note 2): D package	73°C/W
DW package	57°C/W

N package 67°C/W
 NS package 64°C/W
 Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds 260°C
 Storage temperature range, Tstg –65°C to 150°C

Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

2. The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended operating conditions:

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	4.5	5	5.5	V
V _{IH}	High-level input voltage (T1IN, T2IN)	2			V
V _{IL}	Low-level input voltage (T1IN, T2IN)			0.8	V
R1IN, R2IN	Receiver input voltage			±30	V
T _A	Operating free-air temperature	MAX232	0	70	°C
		MAX232I	–40	85	

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 3 and Figure 4)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I _{CC} Supply current	V _{CC} = 5.5 V, All outputs open, T _A = 25°C		8	10	mA

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
 NOTE 3: Test conditions are C1–C4 = 1 μF at V_{CC} = 5 V ± 0.5 V.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (see Note 3)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V _{OH}	High-level output voltage	T1OUT, T2OUT R _L = 3 kΩ to GND	5	7		V
V _{OL}	Low-level output voltage‡	T1OUT, T2OUT R _L = 3 kΩ to GND		-7	-5	V
r _O	Output resistance	T1OUT, T2OUT V _{S+} = V _{S-} = 0, V _O = ±2 V	300			Ω
I _{OS} §	Short-circuit output current	T1OUT, T2OUT V _{CC} = 5.5 V, V _O = 0		±10		mA
I _{IS}	Short-circuit input current	T1IN, T2IN V _I = 0			200	μA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.

§ Not more than one output should be shorted at a time.

NOTE 3: Test conditions are C1–C4 = 1 μF at V_{CC} = 5 V ± 0.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Note 3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Driver slew rate	R _L = 3 kΩ to 7 kΩ, See Figure 2			30	V/μs
SR(t)	Driver transition region slew rate	See Figure 3		3		V/μs
	Data rate	One TOUT switching		120		kbit/s

NOTE 3: Test conditions are C1–C4 = 1 μF at V_{CC} = 5 V ± 0.5 V.

RECEIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (see Note 3)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V _{OH}	High-level output voltage	R1OUT, R2OUT I _{OH} = -1 mA	3.5			V
V _{OL}	Low-level output voltage‡	R1OUT, R2OUT I _{OL} = 3.2 mA			0.4	V
V _{IT+}	Receiver positive-going input threshold voltage	R1IN, R2IN V _{CC} = 5 V, T _A = 25°C		1.7	2.4	V
V _{IT-}	Receiver negative-going input threshold voltage	R1IN, R2IN V _{CC} = 5 V, T _A = 25°C	0.8	1.2		V
V _{hys}	Input hysteresis voltage	R1IN, R2IN V _{CC} = 5 V	0.2	0.5	1	V
r _i	Receiver input resistance	R1IN, R2IN V _{CC} = 5, T _A = 25°C	3	5	7	kΩ

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

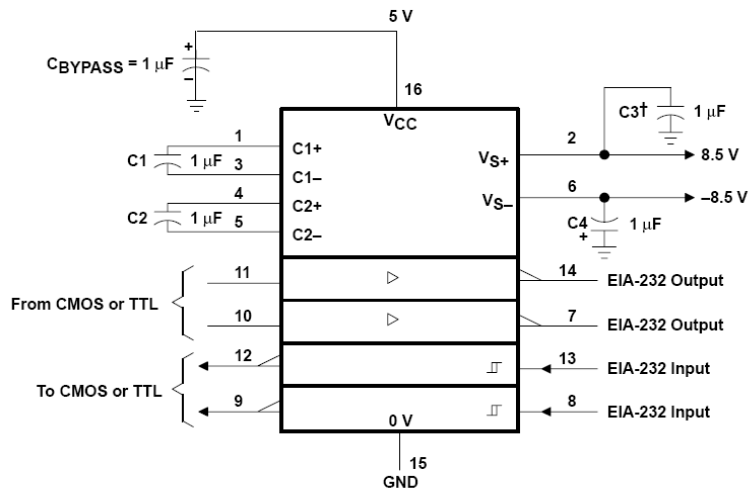
‡ The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.

NOTE 3: Test conditions are C1–C4 = 1 μF at V_{CC} = 5 V ± 0.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Note 3 and Figure 1)

PARAMETER		TYP	UNIT
t _{PLH(R)}	Receiver propagation delay time, low- to high-level output	500	ns
t _{PHL(R)}	Receiver propagation delay time, high- to low-level output	500	ns

NOTE 3: Test conditions are C1–C4 = 1 μF at V_{CC} = 5 V ± 0.5 V.



† C3 can be connected to V_{CC} or GND.

Figure 4. Typical Operating Circuit

IMPORTANT NOTICE

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APPENDIX I operation amplifier datasheet:

ICL7611 datasheet:

The ICL761X/762X/764X series is a family of monolithic CMOS operational amplifiers. These devices provide the designer with high performance operation at low supply voltages and selectable quiescent currents, and are an ideal design tool when ultra low input current and low power dissipation are desired. The basic amplifier will operate at supply voltages ranging from $\sim 1V$ to $\sim 8V$, and may be operated from a single Lithium cell.

A unique quiescent current programming pin allows setting of standby current to 1mA, 100 μ A, or 10 μ A, with no external components. This results in power consumption as low as 20 μ W. The output swing ranges to within a few millivolts of the supply voltages.

Of particular significance is the extremely low (1pA) input current, input noise current of 0.01pA/ $\sqrt{\text{Hz}}$, and 10 $^{12}\Omega$ input impedance. These features optimize performance in very high source impedance applications.

The inputs are internally protected. Outputs are fully protected against short circuits to ground or to either supply. AC performance is excellent, with a slew rate of 1.6V/ μ s, and unity gain bandwidth of 1MHz at $I_Q = 1\text{mA}$. Because of the low power dissipation, junction temperature rise and drift are quite low. Applications utilizing these features may include stable instruments, extended life designs, or high density packages.

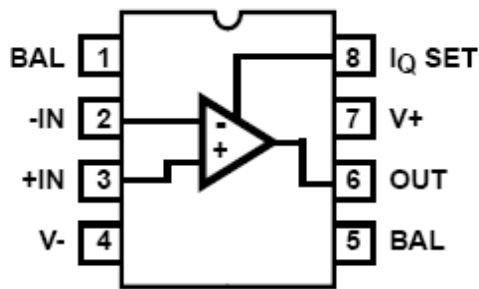
Features

- Wide Operating Voltage Range $\sim 1V$ to $\sim 8V$
- High Input Impedance 10 $^{12}\Omega$
- Programmable Power Consumption. Low as 20 μ W
- Input Current Lower Than BIFETs 1pA (Typ)

- Output Voltage Swing V+ and V-
- Input Common Mode Voltage Range Greater Than Supply Rails (ICL7612)

Applications

- Portable Instruments
- Telephone Headsets
- Hearing Aid/Microphone Amplifiers
- Meter Amplifiers
- Medical Instruments
- High Impedance Buffers



Absolute Maximum Ratings
Thermal Information:

Supply Voltage V+ to

V- 18V

Input Voltage V- -0.3 to V+ +0.3V

Differential Input Voltage (Note 1) [(V+ +0.3) - (V- -0.3)]V

Duration of Output Short Circuit (Note 2) Unlimited

Operating Conditions:

Temperature Range

ICL76XXC 0C⁰ to 70C⁰

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Long term offset voltage stability will be degraded if large input differential voltages are applied for long periods of time.
2. The outputs may be shorted to ground or to either supply, for $V_{SUPPLY} \leq 10V$. Care must be taken to insure that the dissipation rating is not exceeded.
3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $V_{SUPPLY} = \pm 5V$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	ICL7611B, ICL7612B			ICL7611D, ICL7612D			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 100k\Omega$	25	-	-	5	-	-	15	mV
			Full	-	-	7	-	-	20	mV
Temperature Coefficient of V_{OS}	$\Delta V_{OS}/\Delta T$	$R_S \leq 100k\Omega$	-	-	15	-	-	25	-	$\mu V/^\circ C$
Input Offset Current	I_{OS}		25	-	0.5	30	-	0.5	30	pA
			Full	-	-	300	-	-	300	pA
Input Bias Current	I_{BIAS}		25	-	1.0	50	-	1.0	50	pA
			Full	-	-	400	-	-	400	pA
Common Mode Voltage Range (Except ICL7612)	V_{CMR}	$I_Q = 10\mu A$	25	± 4.4	-	-	± 4.4	-	-	V
		$I_Q = 100\mu A$	25	± 4.2	-	-	± 4.2	-	-	V
		$I_Q = 1mA$	25	± 3.7	-	-	± 3.7	-	-	V
Extended Common Mode Voltage Range (ICL7612 Only)	V_{CMR}	$I_Q = 10\mu A$	25	± 5.3	-	-	± 5.3	-	-	V
		$I_Q = 100\mu A$	25	+5.3, -5.1	-	-	+5.3, -5.1	-	-	V
		$I_Q = 1mA$	25	+5.3, -4.5	-	-	+5.3, -4.5	-	-	V
Output Voltage Swing	V_{OUT}	$I_Q = 10\mu A, R_L = 1M\Omega$	25	± 4.9	-	-	± 4.9	-	-	V
			Full	± 4.8	-	-	± 4.8	-	-	V
		$I_Q = 100\mu A, R_L = 100k\Omega$	25	± 4.9	-	-	± 4.9	-	-	V
			Full	± 4.8	-	-	± 4.8	-	-	V
		$I_Q = 1mA, R_L = 10k\Omega$	25	± 4.5	-	-	± 4.5	-	-	V
			Full	± 4.3	-	-	± 4.3	-	-	V
Large Signal Voltage Gain	A_{VOL}	$V_O = \pm 4.0V, R_L = 1M\Omega, I_Q = 10\mu A$	25	80	104	-	80	104	-	dB
			Full	75	-	-	75	-	-	dB
		$V_O = \pm 4.0V, R_L = 100k\Omega, I_Q = 100\mu A$	25	80	102	-	80	102	-	dB
			Full	75	-	-	75	-	-	dB
		$V_O = \pm 4.0V, R_L = 10k\Omega, I_Q = 1mA$	25	76	83	-	76	83	-	dB
			Full	72	-	-	72	-	-	dB

Electrical Specifications $V_{SUPPLY} = \pm 5V$, Unless Otherwise Specified (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	ICL7611B, ICL7612B			ICL7611D, ICL7612D			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
Unity Gain Bandwidth	GBW	$I_Q = 10\mu A$	25	-	0.044	-	-	0.044	-	MHz
		$I_Q = 100\mu A$	25	-	0.48	-	-	0.48	-	MHz
		$I_Q = 1mA$	25	-	1.4	-	-	1.4	-	MHz
Input Resistance	R_{IN}		25	-	10^{12}	-	-	10^{12}	-	Ω
Common Mode Rejection Ratio	CMRR	$R_S \leq 100k\Omega, I_Q = 10\mu A$	25	70	96	-	70	96	-	dB
		$R_S \leq 100k\Omega, I_Q = 100\mu A$	25	70	91	-	70	91	-	dB
		$R_S \leq 100k\Omega, I_Q = 1mA$	25	60	87	-	60	87	-	dB
Power Supply Rejection Ratio ($V_{SUPPLY} = \pm 8V$ to $\pm 2V$)	PSRR	$R_S \leq 100k\Omega, I_Q = 10\mu A$	25	80	94	-	80	94	-	dB
		$R_S \leq 100k\Omega, I_Q = 100\mu A$	25	80	86	-	80	86	-	dB
		$R_S \leq 100k\Omega, I_Q = 1mA$	25	70	77	-	70	77	-	dB
Input Referred Noise Voltage	e_N	$R_S = 100\Omega, f = 1kHz$	25	-	100	-	-	100	-	nV/\sqrt{Hz}
Input Referred Noise Current	i_N	$R_S = 100\Omega, f = 1kHz$	25	-	0.01	-	-	0.01	-	pA/\sqrt{Hz}
Supply Current (No Signal, No Load)	I_{SUPPLY}	I_Q SET = +5V, Low Bias	25	-	0.01	0.02	-	0.01	0.02	mA
		I_Q SET = 0V, Medium Bias	25	-	0.1	0.25	-	0.1	0.25	mA
		I_Q SET = -5V, High Bias	25	-	1.0	2.5	-	1.0	2.5	mA
Channel Separation	V_{O1}/V_{O2}	$A_V = 100$	25	-	120	-	-	120	-	dB
Slew Rate ($A_V = 1, C_L = 100pF, V_{IN} = 8V_{P-P}$)	SR	$I_Q = 10\mu A, R_L = 1M\Omega$	25	-	0.016	-	-	0.016	-	$V/\mu s$
		$I_Q = 100\mu A, R_L = 100k\Omega$	25	-	0.16	-	-	0.16	-	$V/\mu s$
		$I_Q = 1mA, R_L = 10k\Omega$	25	-	1.6	-	-	1.6	-	$V/\mu s$
Rise Time ($V_{IN} = 50mV, C_L = 100pF$)	t_r	$I_Q = 10\mu A, R_L = 1M\Omega$	25	-	20	-	-	20	-	μs
		$I_Q = 100\mu A, R_L = 100k\Omega$	25	-	2	-	-	2	-	μs
		$I_Q = 1mA, R_L = 10k\Omega$	25	-	0.9	-	-	0.9	-	μs
Overshoot Factor ($V_{IN} = 50mV, C_L = 100pF$)	OS	$I_Q = 10\mu A, R_L = 1M\Omega$	25	-	5	-	-	5	-	%
		$I_Q = 100\mu A, R_L = 100k\Omega$	25	-	10	-	-	10	-	%
		$I_Q = 1mA, R_L = 10k\Omega$	25	-	40	-	-	40	-	%

Electrical Specifications $V_{SUPPLY} = \pm 1V, I_Q = 10\mu A$, Unless Otherwise Specified

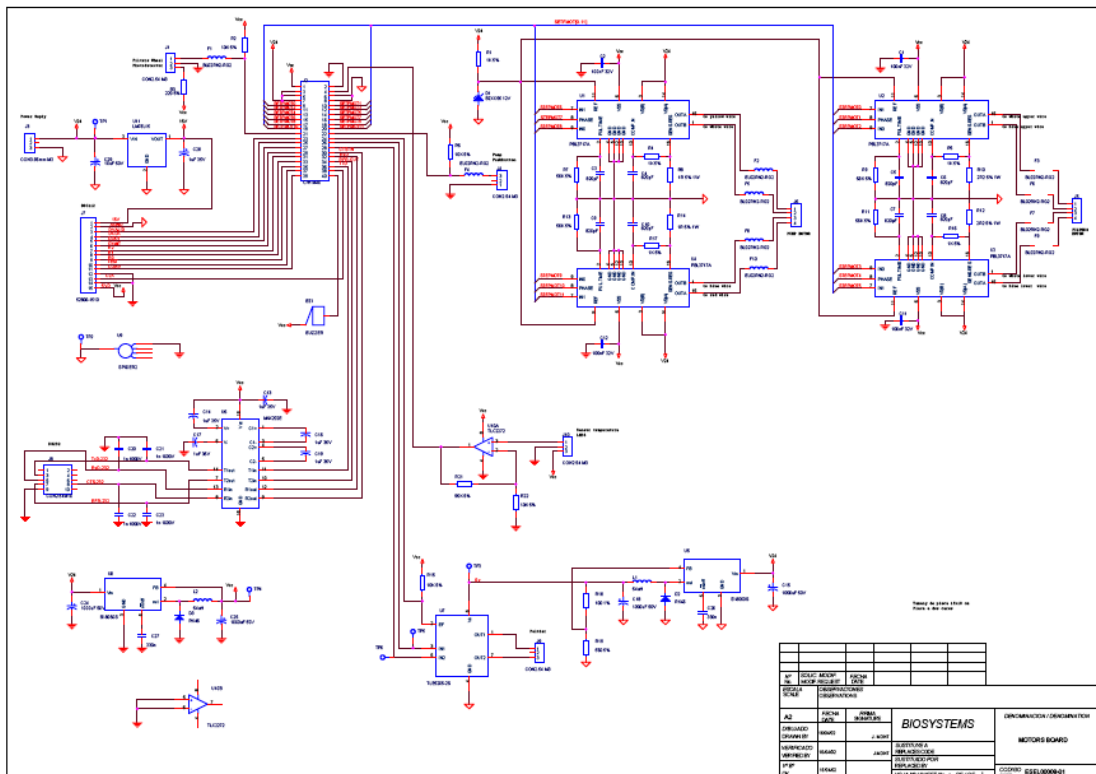
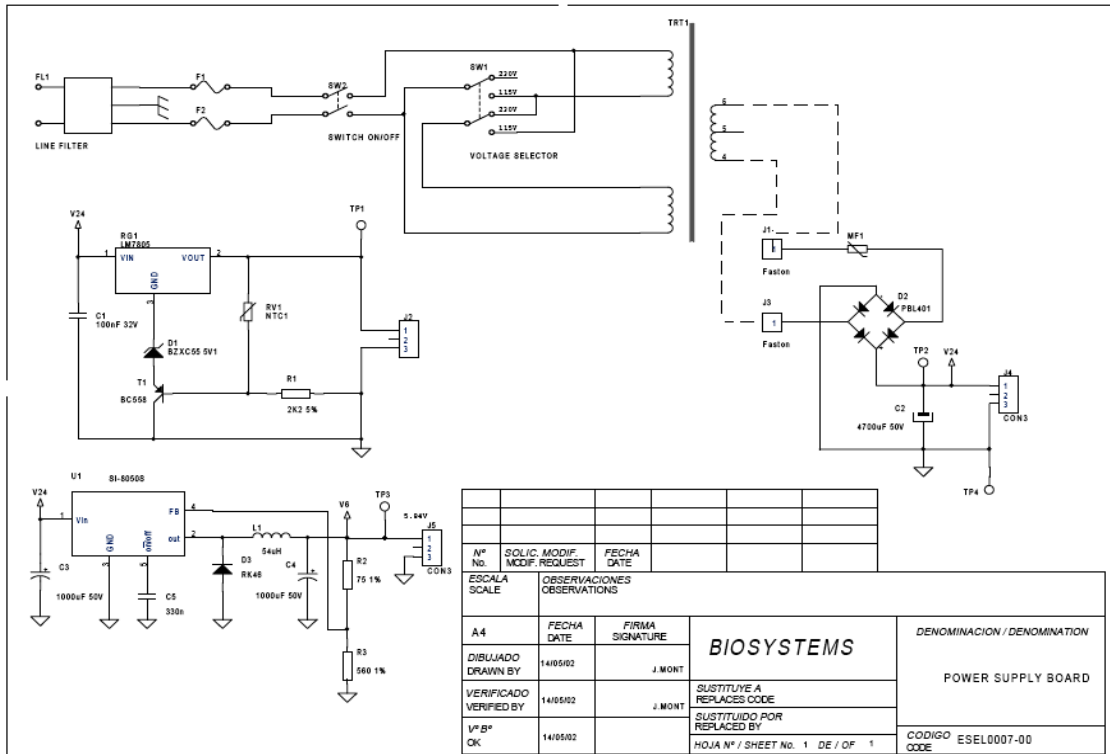
PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	ICL7611B, ICL7612B			UNITS
				MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 100k\Omega$	25	-	-	5	mV
			Full	-	-	7	mV
Temperature Coefficient of V_{OS}	$\Delta V_{OS}/\Delta T$	$R_S \leq 100k\Omega$	-	-	15	-	$\mu V/^\circ C$
Input Offset Current	I_{OS}		25	-	0.5	30	pA
			Full	-	-	300	pA
Input Bias Current	I_{BIAS}		25	-	1.0	50	pA
			Full	-	-	500	pA
Common Mode Voltage Range (Except ICL7612)	V_{CMR}		25	± 0.6	-	-	V

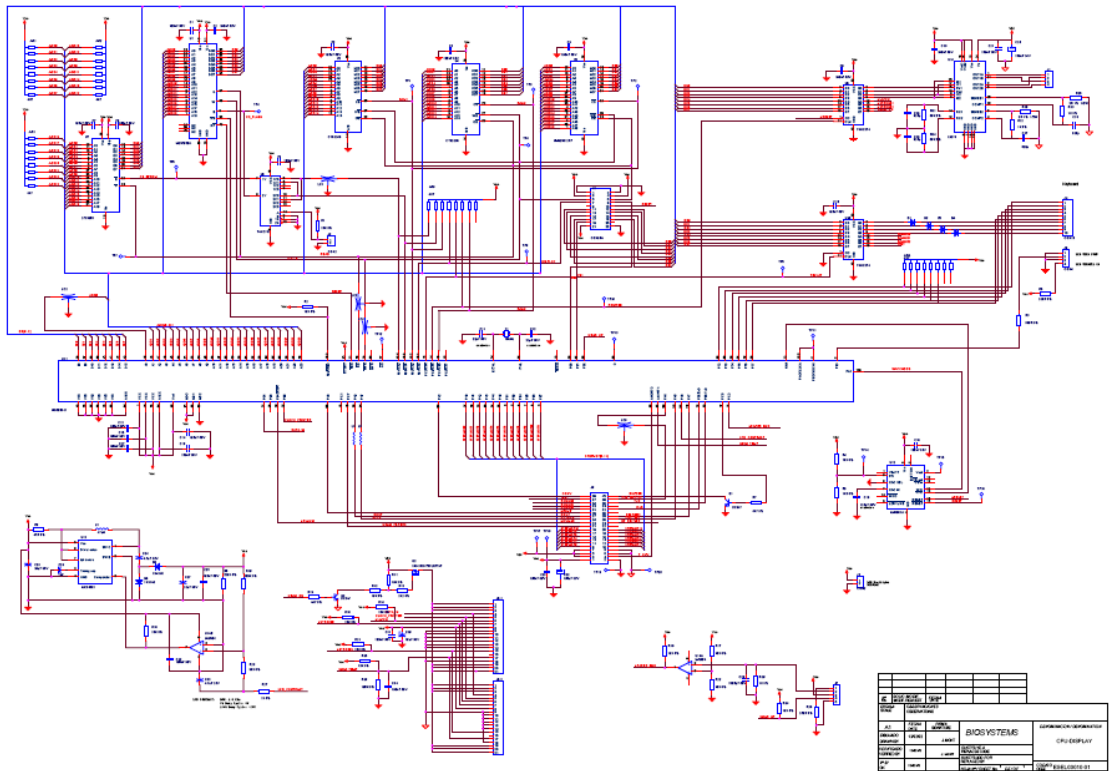
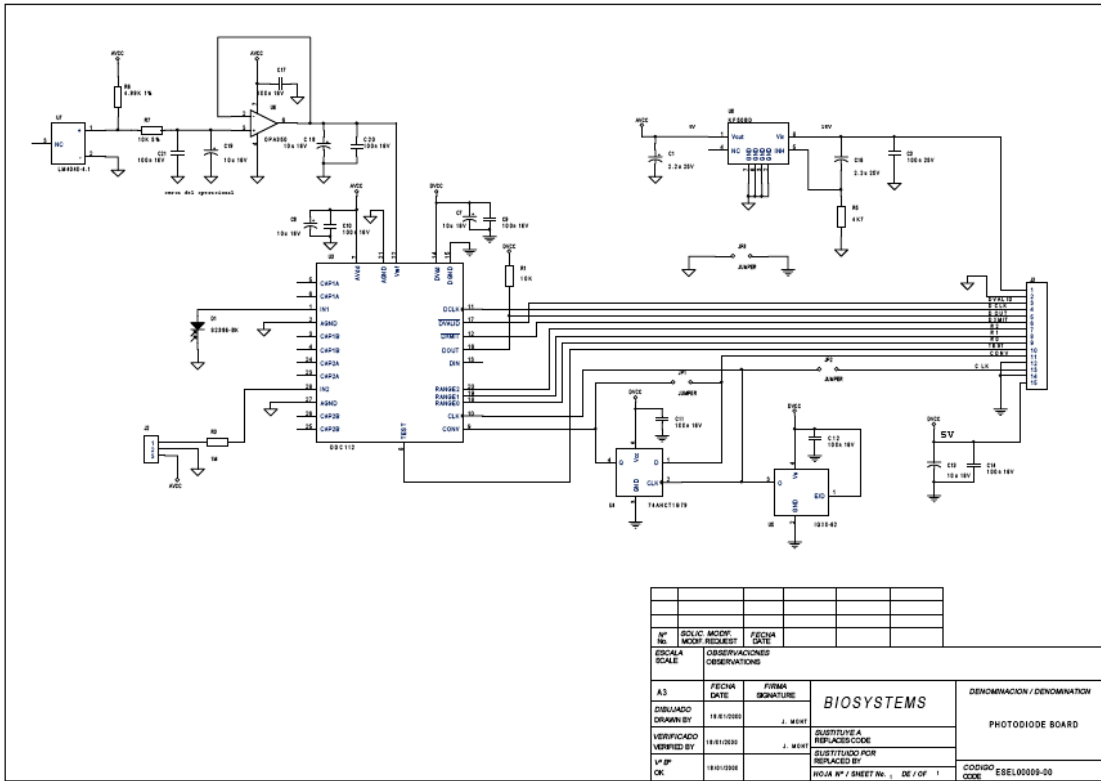
Electrical Specifications $V_{\text{SUPPLY}} = \pm 1\text{V}$, $I_{\text{Q}} = 10\mu\text{A}$, Unless Otherwise Specified (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	ICL7611B, ICL7612B			UNITS
				MIN	TYP	MAX	
Extended Common Mode Voltage Range (ICL7612 Only)	V_{CMR}		25	+0.6 to -1.1	-	-	V
Output Voltage Swing	V_{OUT}	$R_{\text{L}} = 1\text{M}\Omega$	25	± 0.98	-	-	V
			Full	± 0.96	-	-	V
Large Signal Voltage Gain	A_{VOL}	$V_{\text{O}} = \pm 0.1\text{V}$, $R_{\text{L}} = 1\text{M}\Omega$	25	-	90	-	dB
			Full	-	80	-	dB
Unity Gain Bandwidth	GBW		25	-	0.044	-	MHz
Input Resistance	R_{IN}		25	-	10^{12}	-	Ω
Common Mode Rejection Ratio	CMRR	$R_{\text{S}} \leq 100\text{k}\Omega$	25	-	80	-	dB
Power Supply Rejection Ratio	PSRR	$R_{\text{S}} \leq 100\text{k}\Omega$	25	-	80	-	dB
Input Referred Noise Voltage	e_{N}	$R_{\text{S}} = 100\Omega$, $f = 1\text{kHz}$	25	-	100	-	$\text{nV}/\sqrt{\text{Hz}}$
Input Referred Noise Current	i_{N}	$R_{\text{S}} = 100\Omega$, $f = 1\text{kHz}$	25	-	0.01	-	$\text{pA}/\sqrt{\text{Hz}}$
Supply Current	I_{SUPPLY}	No Signal, No Load	25	-	6	15	μA
Slew Rate	SR	$A_{\text{V}} = 1$, $C_{\text{L}} = 100\text{pF}$, $V_{\text{IN}} = 0.2\text{V}_{\text{P-P}}$, $R_{\text{L}} = 1\text{M}\Omega$	25	-	0.016	-	$\text{V}/\mu\text{s}$
Rise Time	t_{r}	$V_{\text{IN}} = 50\text{mV}$, $C_{\text{L}} = 100\text{pF}$, $R_{\text{L}} = 1\text{M}\Omega$	25	-	20	-	μs
Overshoot Factor	OS	$V_{\text{IN}} = 50\text{mV}$, $C_{\text{L}} = 100\text{pF}$, $R_{\text{L}} = 1\text{M}\Omega$	25	-	5	-	%

APPENDIX J the Wavelengths of absorbed and observed colors:

Solution color	Absorbed color	λ absorbed (nm)
Green-Yellow	Violet	380-420
Yellow	Violet-blue	420-440
Orange	Blue	440-470
Red	Blue-Green	470-500
Purple-Red	Green	500-520
Violet	Yellow-Green	520-550
Violet-Blue	Yellow	550-580
Blue	Orange	580-620
Blue-Green	Red	620-680
Gree	Red	680-780





APPENDIX K normal and pathological reading

Normal reading

	Phosph ate	Ure a	Uri c aci d	Albu min	Gluco se	Control Phosph ate	Cont rol Urea	Cont rol Uric acid	Contr ol Albu min	C o n t r o l G l u c o s e
1	7.30	26.0 0	6.4 0	28.00	90.50	7.31	26.70	5.93	24.90	86 .5 0
2	7.32	26.4 0	5.8 0	20.50	74.20	7.31	26.70	5.93	24.90	86 .5 0
3	7.36	24.0 0	6.2 0	27.80	86.50	7.31	26.70	5.93	24.90	86 .5 0
4	6.90	26.5 0	6.3 0	26.00	74.00	7.31	26.70	5.93	24.90	86 .5 0
5	7.35	26.7 0	5.2 0	26.50	92.30	7.31	26.70	5.93	24.90	86 .5

6	7.80	29.65	6.45	28.80	88.60	7.31	26.70	5.93	24.90	86.50
7	7.37	26.40	6.56	27.00	75.50	7.31	26.70	5.93	24.90	86.50
8	7.00	23.40	5.30	26.00	98.50	7.31	26.70	5.93	24.90	86.50
9	7.00	26.50	6.89	27.00	75.90	7.31	26.70	5.93	24.90	86.50
10	10.00	26.50	6.90	26.50	99.00	7.31	26.70	5.93	24.90	86.50

Pathological reading

	Phosph ate	Ure a	Uric aci d	Albu min	Gluco se	Control Phosph ate	Cont rol Urea	Cont rol Uric acid	Contr ol Albu min	Con trol Glu cos e
1	35.90	20.50	9.60	37.50	12.90	22.90	25.80	37.50	9.68	14.70

2	25.50	22.90	9.00	30.90	14.70	22.90	25.80	37.50	9.68	14.70
3	25.50	19.50	9.60	44.00	14.00	22.90	25.80	37.50	9.68	14.70
4	38.50	26.00	8.50	37.50	16.90	22.90	25.80	37.50	9.68	14.70
5	13.00	22.90	9.60	30.80	15.00	22.90	25.80	37.50	9.68	14.70
6	25.50	24.50	10.50	35.00	14.70	22.90	25.80	37.50	9.68	14.70
7	30.00	23.00	9.60	39.50	16.50	22.90	25.80	37.50	9.68	14.70
8	25.50	22.90	11.00	38.00	14.90	22.90	25.80	37.50	9.68	14.70
9	33.50	25.50	10.50	40.50	15.50	22.90	25.80	37.50	9.68	14.70
10	25.50	22.90	8.50	37.50	14.70	22.90	25.80	37.50	9.68	14.70

APPENDIX L Bio-system reagent datasheet