

السودان

**Sudan University of Science and Technology**

**College of Engineering**

**Department of Electronics**

**Design and Simulation of Digital Down Converter for  
Software-Defined Radio (SDR)**

السودان

A thesis submitted in partial fulfilment of the requirements for the degree of  
Master of Science in Telecommunication Engineering

**Prepared By: Mussab Hussien Ali**

**Supervised By: Dr. Mohammad Ali Hamad Abbas**

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## **ABSTRACT**

A digital down converter is one of the main parts of the software defined radio, to enable driving the signal from antenna to the baseband processing which was till the recent past too difficult due to less reliability of processing and analog circuitry. Nowadays high frequency processing is in demand with the appearance of FPGA, and ASIC. The digital and very high speed processing have become more available.

In this thesis full design and simulation of the digital down converter (DDC) is done. The simulation took two paths, MATLAB path and VHDL path. In the MATLAB path SIMULINK blocks were used to represent the DDC parts, two quadrature signals with very high data rate (about 140 Mbps) inputs to the DDC mixer, then numerically controlled oscillator (NCO) block parameters were set to generate an appropriate local oscillator (LO) frequency and mixed with the quadrature signals to get suitable intermediate frequency, Then a chain of FIR CIC filters is used to down convert the high rate and separate the base band signal.

The VHDL path follows the MATLAB model. In Xilinx SIMULINK block set, the system generator block is used to convert MATLAB model to VHDL code, Test bench file is generated and modified to satisfy the design parameters. Compilation and simulation of the code have been done.

The final signal information and data rate obtained from the MATLAB has been compared to VHDL results, The input RF signal was 299 Mhz and after DDC is become 675 Khz and the sample rate was down converted from 140 Mbps to 2.187 Mbps and the compared results were identical.



يعتبر مخفض التردد الرقمي جزءاً أساسياً من أجزاء الراديو المعرف برمجياً، للتمكين من جلب الإشارة من الهوائي الي عمليات النطاق الأدنى التي كانت حتى وقت قريب صعبة للغاية وذلك لقلة اعتمادية العمليات والدوائر التماثلية. وصارت في هذه الايام معالجة الترددات العالية مطلوبة مع ظهور مصفوفات البوابات المبرمجة حقلياً (FPGA) والدوائر المتكاملة المحددة التطبيق (ASIC)، واصبحت المعالجة الرقمية والسريعة جداً متاحة أكثر.

في هذا البحث تم عمل محاكاة كاملة لمخفض التردد الرقمي، وقد أخذت المحاكاة مسارين: مسار برنامج الماتلاب ومسار لغة وصف العتاد الصلب. في مسار الماتلاب تم استخدام القطع الجاهزة المتوفرة ببرنامج SIMULINK لتمثيل أجزاء مخفض التردد الرقمي. تم ادخال اشارتين بينهما تعامد في الطور بمعدل بيانات عال جداً (تقريباً 140 Mb/s) للمازج ثم تم ضبط معاملات المذبذب المتحكم به رقمياً لتوليد تردد محلي معين مُزج مع الإشارتين للحصول على تردد وسيط مناسب، ثم تم استخدام المرشحات المشطية المكاملة المتسلسلة لخفض معدل البيانات وعزل إشارة النطاق الأدنى.

مسار لغة وصف العتاد الصلب يتبع نموذج الماتلاب. حيث تم استخدام قطعة مولد النظام الموجودة مع قطع شركة (زيلنكس) لتحويل نموذج الماتلاب الى رموز لغة وصف العتاد الصلب، وتم توليد وتعديل برنامج الأختبار ليناسب معاملات التصميم ثم تم تشغيل ومحاكاة البرنامج.

أخيراً تم الحصول على معلومات الإشارة ومعدل البيانات النهائي من نموذج الماتلاب ومقارنتها مع نتائج لغة وصف العتاد الصلب، حيث تم ادخال إشارة رادية 299 ميغاهيرتز وبعد

أستخدام مخفض التردد الرقمي كانت الاشارة 675 كيلوهيرتز، وتم خفض معدل البيانات من 140 Mb/s الى 2.187 Mb/s وكانت نتيجة المقارنة متطابقة.

## Abbreviations

AC	Alternate Current
ADC	Analog to Digital Converter
ASIC	Application Specific Integrated Circuit
BPF	Band Pass Filter
BW	Band Width
CFIR	Compensation Finite Impulse Response
CIC	Cascade Integrator Comb
CORDIC	Coordinate Rotation Digital Computer
DAC	Digital to Analog Converter
DB	Decibel
DDC	Digital Down Converter
DDS	Direct Digital Synthesizer
DSP	Digital Signal Processor
DSS	Digitally Synthesized Source
DUC	Digital Up Converter
FCW	Frequency Control Word
FIR	Finite Impulse Response

FM	Frequency Modulation
FPGA	Field-Programmable Gate Array
FTW	Frequency Tuning Word
GCD	Greatest Common Divisor
Ghz	Giga Hertz
HBF	Half Band Filter
HDL	Hardware Description Language
HDR	Hardware Defined Radio
Hz	Hertz
IC	Integrated Circuit
IF	Intermediate Frequency
IIR	Infinite Impulse Response
IP	Intellectual Property
IQ	In-phase Quadrature-phase
ISE	Integrated Synthesis Environment
ISIM	ISE Simulator
Khz	Kilo Hertz
LNA	Low Noise Amplifier
LO	Local Oscillator
LPF	Low Pass Filter
LSB	Least Significant Bit
LUT	Look-Up Table
MAC	Media Access Control
Mhz	Mega Hertz

MODEM	Modulator/Demodulator
MSB	Most Significant Bit
MSPS	Million Sample Per Second
NCO	Numerically Controlled Oscillator
ns	Nano Second
PA	Phase Accumulator
PAC	Phase-to-Amplitude Converter
PFIR	Programmable Finite Impulse Response
PLL	Phased Locked Loop
PPC	Point Per Clock
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RMS	Root Mean Square
ROM	Random Access Memory
RTL	Register Transfer Level
SAW	Surface Acoustic Wave
SDR	Software-Defined Radio
Sec	Second
SFDR	Spurious-Free Dynamic Range
SNR	Signal-to-Noise Ratio
VCO	Voltage Control Oscillator
VHDL	Very High Speed Description Language
VLSI	Very Large Scale Integrated Circuit

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