

HD74LS373

Octal D-type Transparent Latches (with three-state outputs)

The HD74LS373, 8-bit register features totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide this register with the capacity of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

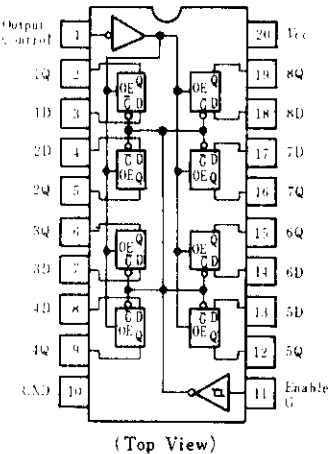
The eight latches are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was setup.

FUNCTION TABLE

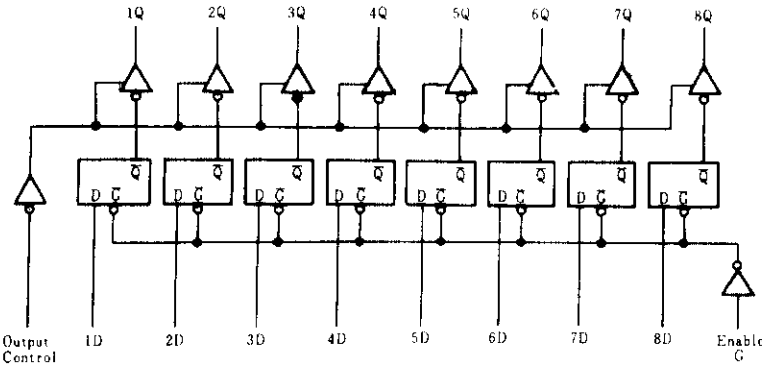
Inputs			Output
Output control	Enable G	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q ₀
H	X	X	Z

Notes: H = high level, L = low level,
X = irrelevant
Q₀ = level of Q before the indicated steady-state input conditions were established.
Z = off (high-impedance) state of a three-state output

PIN ARRANGEMENT



BLOCK DIAGRAM

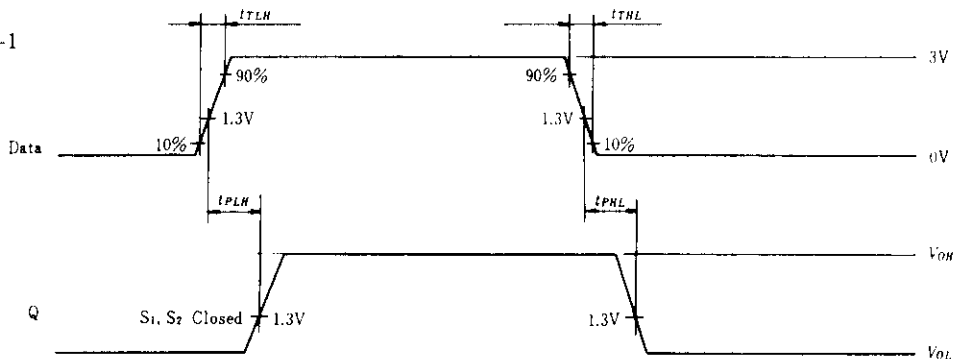


RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Supply voltage	V _{CC}	4.75	5.00	5.25	V
Output voltage	V _{OH}	—	—	5.5	V
Output current	I _{OH}	—	—	—2.6	mA
	I _{OL}	—	—	24	mA
Enable pulse width	t _w	15	—	—	ns
		15	—	—	ns
Data setup time	t _{su}	5 ↓	—	—	ns
Data hold time	t _h	25 ↓	—	—	ns

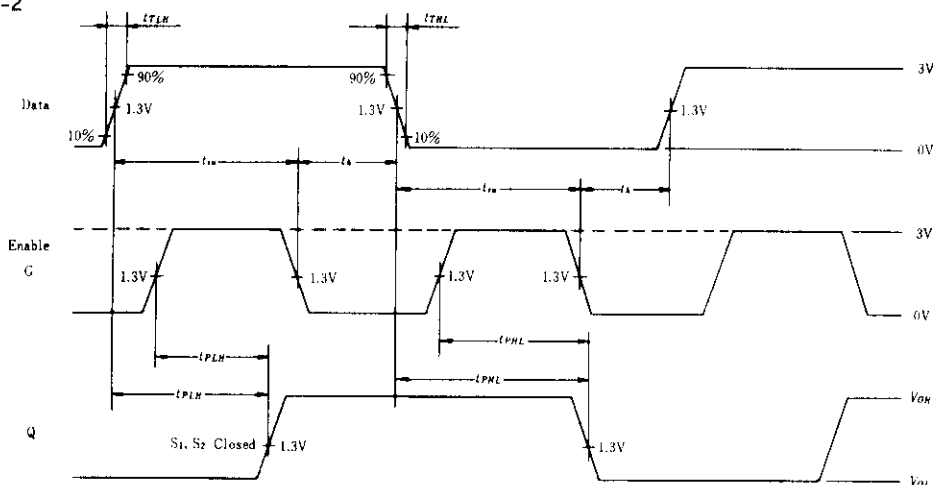
Note) ↓ : The arrow indicates the falling edge of clock pulse.

Waveform-1



Notes: Input pulse; $t_{TLH} \leq 15ns$, $t_{THL} \leq 6ns$, $PRR = 1MHz$, duty cycle 50%

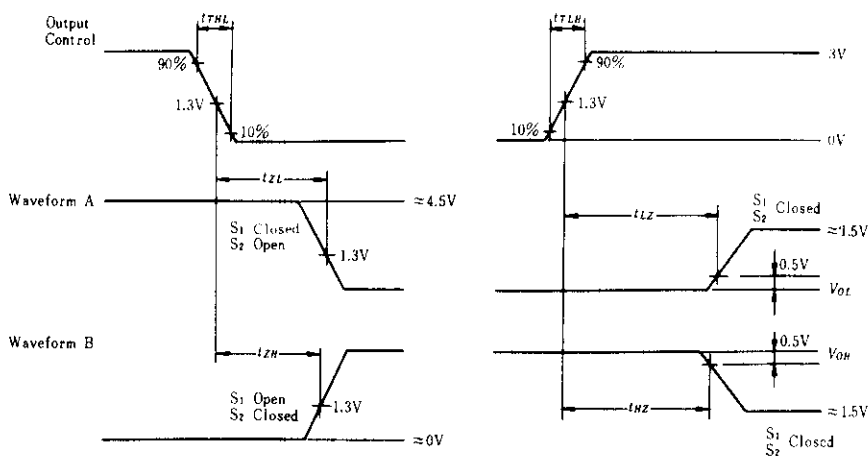
Waveform-2



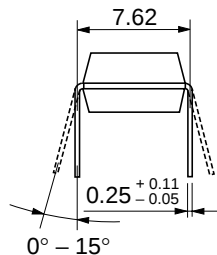
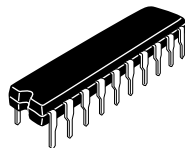
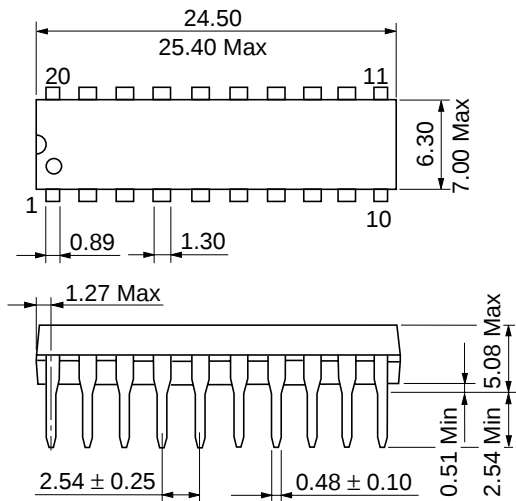
Note: Enable input pulse; $t_{TLH} \leq 15ns$, $t_{THL} \leq 6ns$, $PRR = 1MHz$

Data input pulse; $t_{TLH} \leq 15ns$, $t_{THL} \leq 6ns$, $PRR = 1MHz$, G input is high.

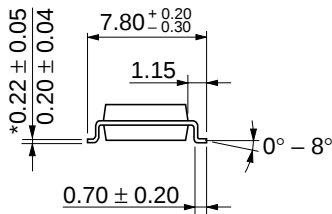
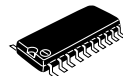
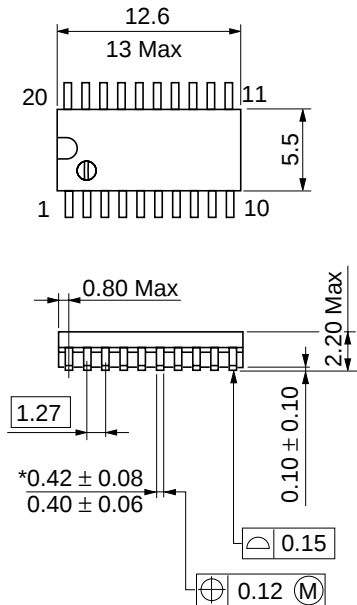
Waveform-3



Notes: 1. Input pulse; $t_{TLH} \leq 15ns$, $t_{THL} \leq 6ns$, $PRR = 1MHz$, duty cycle 50%
2. Waveform A if for an output with internal conditions such that the output is low except when disabled by the output control. Waveform B is for an output with internal conditions such that the output is high except when disabled by the output control.

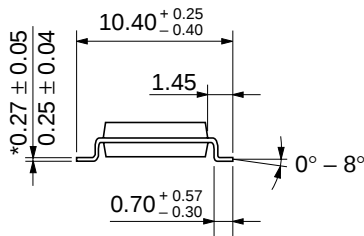
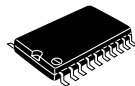
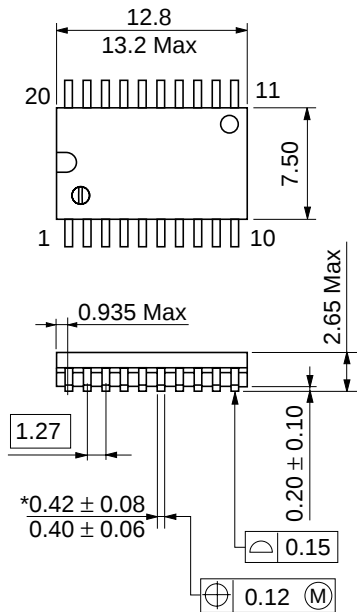


Hitachi Code	DP-20N
JEDEC	—
EIAJ	Conforms
Weight (reference value)	1.26 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-20DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.31 g



Hitachi Code	FP-20DB
JEDEC	Conforms
EIAJ	—
Weight (reference value)	0.52 g

*Dimension including the plating thickness
Base material dimension

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