Appendix C

ATmega 16 and ATmega 16L Data sheet

C.1 Features

- High – performance, low – power AVR® 8- bit microcontroller.
- Advanced RISC architecture.
    - 131 powerful instruction – most single – clock cycle executions.
    - 32×8 general purpose working registers.
    - Fully static operation.
    - Up to 16 MIPS throughput at 16 M_{HZ}.
    - On – chip 2 – cycle multiplier.
- Non-volatile program and data memories
    - 16K byte of in – system self – programmable flash endurance: 10,000 Write/Erase cycles.
    - Optional boot code section with independent lock bits in – system programming by on – chip boot program true read – while – write operation.
    - 512 bytes EEPROM. Endurance: 100,000 write/erase cycles.
    - 1K byte internal SRAM.
    - Programmings lock for software security.
- JTAG (IEEE std. 1149.1 compliant) interface.
    - Boundary – scan capabilities according to the JTAG standard.
    - Extensive on – chip debug support.
    - Programming of flash, EEPROM, fuses, and lock bits through the JTAG interface.

- Peripheral features
  - Two 8 – bit timer/counters with separate prescalers and compare modes.
  - One 16 – bit timer/counter with separate prescalers, compare mode, and capture mode.
  - Real time counters with separate oscillator.
  - Four PWM channels.
  - 8 – Channel, 10 – bit ADC.

    8 single – ended channels.

    7 differential channels in TQFP package only.

    2 differential channels with programmable gain at 1x, 10x, or 200x.
  - Byte – oriented two – wire serial interface.
  - Programmable serial USART.
  - Master/Slave SPI serial interface.
  - Programmable watchdog timer with separate on – chip oscillator.
  - On – chip Analog comparator.
- Special microcontroller features
  - Power – on reset and programmable brown – out detection.
  - Internal calibrated RC oscillator.
  - External and internal interrupt sources.
  - Six sleep modes : Idle, ADC noise reduction, power – save , power – down, standby,
- I/O and packages
  - 32 programmable I/O lines.
  - 40 – Pin PDIP, 44 – lead TQFP, and 44 – pad MLF.

- Operating voltages
  - 2.7 – 5.5V for Atmega16L.
  - 4.5 – 5.5V for Atmega16L.
- Speed Grades
  - 0 – 8 M_{HZ} for Atmega16L.
  - 0 – 16 M_{HZ} for Atmega16L.
- Power consumption at 1 M_{HZ} , 3V, and 25 °C for Atmega16L
  - Active: 1.1 mA.
  - Idle mode: 0.35 mA.
  - Power – down mode: < 1µA.

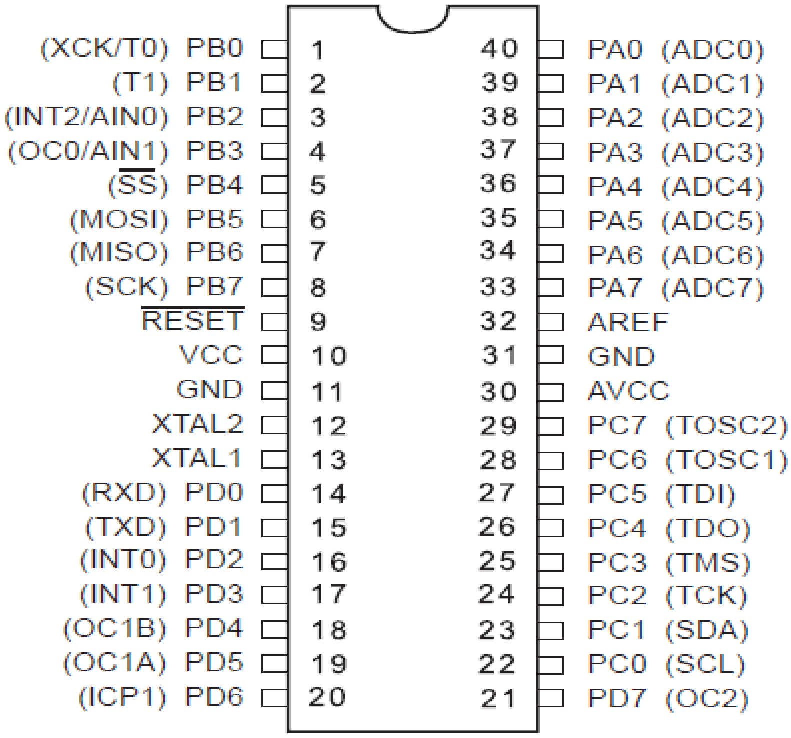


Figure c.1: Pinouts Atmega16 (PDIP)

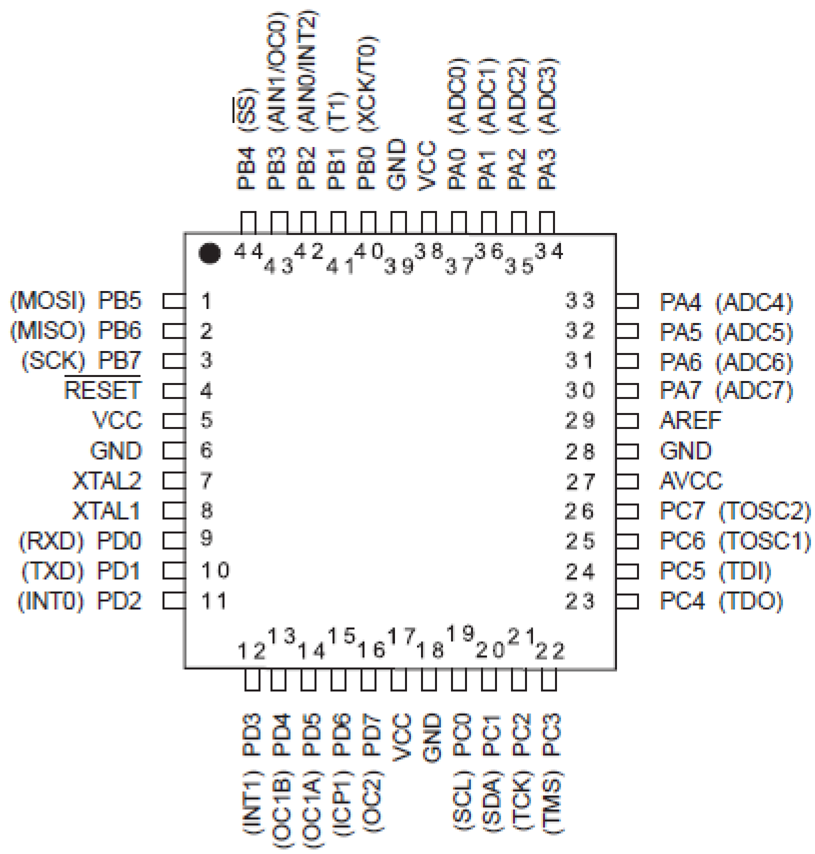


Figure c.2: Pinouts Atmega16 (TQFP/MLF)

C.2 Disclaimer

Typical values contained in this datasheet are based on simulations and char – acterization of other AVR microcontrollers manufactured on the same process technology. Min and Max values will be available after the device is characte-rized.

C.3 Overview

The Atmega16 is a low – power CMOS 8 – bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the Atmega16 achieves throughputs approaching 1 MIPS per MH_Z allowing the system designer to optimize power consumption versus processing speed.

C.4 Block Diagram

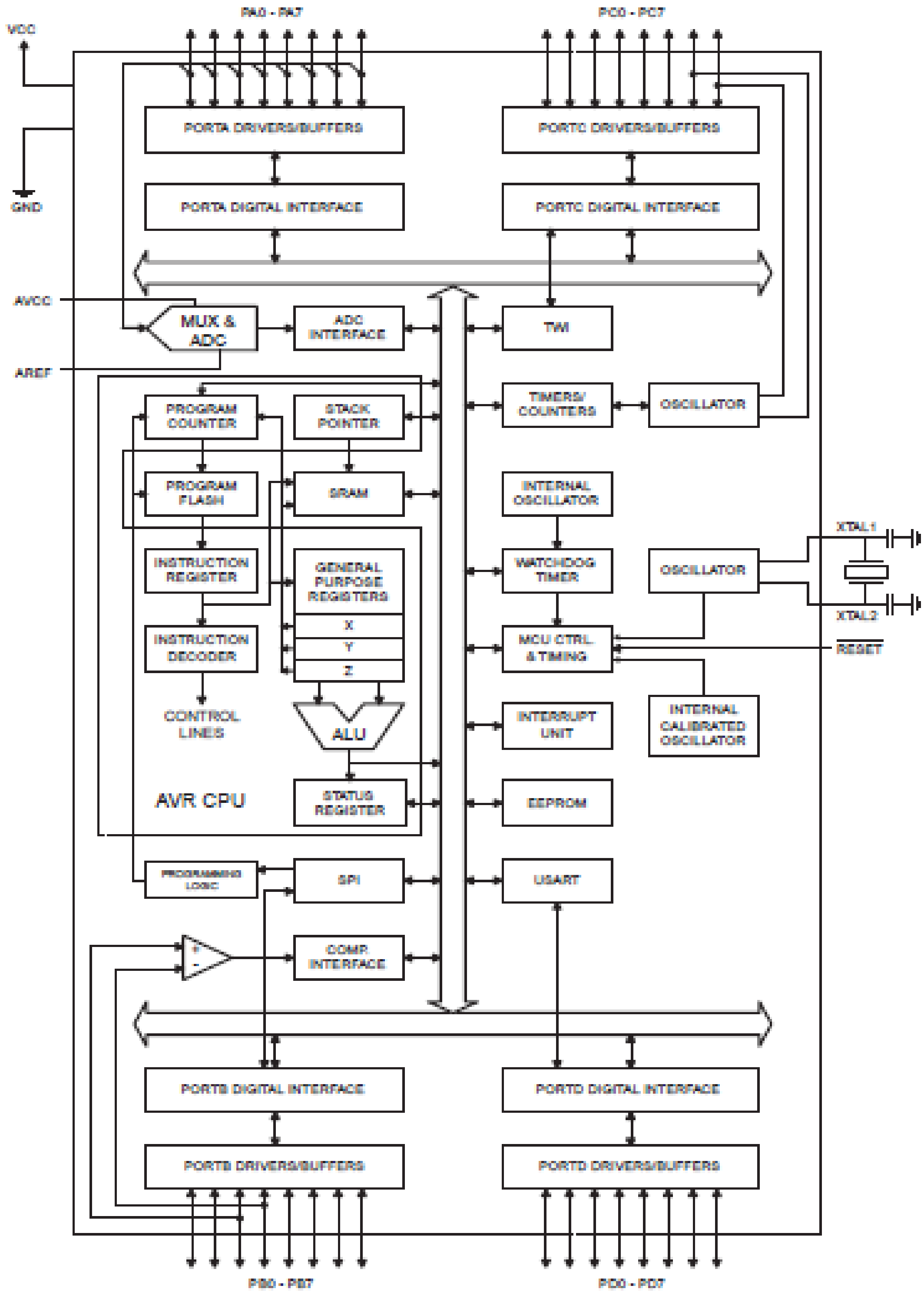


Figure c.3: Block Diagram

The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontroller.

The Atmega16 provides the following features: 16K bytes of in – system Programmable flash program memory with Read-While-Write capabilities, 512 bytes EEPROM, 1K byte SRAM, 32 general purpose I/O lines, 32 general purpose working registers, a JTAG interface for boundary – scan, On-chip debugging support and programming, three flexible Timer/Counters with compare modes, internal and external interrupts, a serial programmable USART, a byte oriented Two – wire serial interface, an 8 – channel, 10 – bit ADC with optional differential input stage with programmable gain (TQFP package only), a programmable watchdog timer with internal oscillator, an SPI serial port, and six software selectable power saving modes. The IDIE mode stops the CPU while allowing the USART, Two – wire interface, A/D converter, SRAM, Timer/Counters, SPI port, and interrupt system to continue functioning. The power – down mode saves the register contents but freezes the oscillator, disabling all other chip functions unit the next external interrupt or hardware reset. In power save mode, the asynchronous Timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC noise reduction mode stops the CPU and all I/O modules except asynchronous Timer and ADC, to minimize switching noise during ADC conversions. In standby mode, the crystal/resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start- up combined with low- power consumption. In extended standby mode, both the main oscillator and the asynchronous Timer continue to run.

The device is manufactured using Atmel's high density non-volatile memory technology the on- chip ISP flash allows the program memory to be reprogrammed in- system through an SPI serial interface, by a conventional non-volatile memory programme, or by an on- chip boot program running on the AVR core. The boot program can use any interface to download the application program in the application flash memory software in the boot flash section will continue to run while the application flash section is updated, providing true Read-While-Write operation. By combining an 8- bit RISC CPU with in- system self- programmable flash on a monolithic chip, the Atmel Atmega16 is a powerful microcontroller that provides a highly-flexible and cost- effective solution to many embedded control applications.

The Atmega16 AVR is supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, in- circuit emulators, and evaluation kits.

C.5 Pin Description

VCC: Digital supply voltage

GND: Ground.

Port A (PA0- PA7): Port A serves as the analog inputs to the A/D Converter. Also port A serves as an 8-bit bi-directional input/output (I/O) port, if the A/D converter is not used.

Port B (PB0- PB7): Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit).

Port C (PC0- PC7): Port C is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit).

Port D (PD0- PD7): Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit).

RESET: A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running.

XTAL1: Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2: Output from the inverting oscillator amplifier.

AVCC: AVCC is the supply voltage pin for port A and the A/D converter. It should be externally connected to VCC, even if the ADC is not used. If the ADC is used, it should be connected to VCC through a low-pass filter.

AREF: is the analog reference pin for the A/D converter.

Appendix D

2^{12} Series of Encoders Data Sheet

D.1 Features

- Operating voltage
  - 2.4V ~ 5V for the HT12A
  - 2.4V ~ 12V for the HT12E
- Low power and high noise immunity CMOS technology
- Low standby current: 0.1µA (typ.) at V_{DD}= 5V
- HT12A with a 38KH_Z carrier for infrared transmission medium
- Minimum transmission word
  - Four word for the HT12E
  - One word for the HT12A
- Built – in oscillator needs only 5% resistor
- Data code has positive polarity
- Minimal external components
- HT12A/E: 18-pin DIP/20-pin SOP package

D.2 Applications

- Burglar alarm system.
- Smoke and fire alarm system.
- Garage door controllers.
- Car alarm system.
- Security system.
- Cordless telephone.
- Other remote control system.

D.3 General Description

The 2^{12} encoders are a serial of CMOS LSIs for remote control system applications. They are capable of encoding information which consists of N address bits and 12 – N data bits. Each address/data input can be set to one of the two logic states. The programmed address/data are transmitted together with the header bits via an RF or an infrared transmission medium upon receipt of a trigger signal. The capability to select a TE trigger on the HT12E or a data trigger on the HT12A further enhances the application flexibility of the 2^{12} series of encoders. The HT12A additionally provides a 38 kHz carrier for infrared system.

Table D.1: selection general description

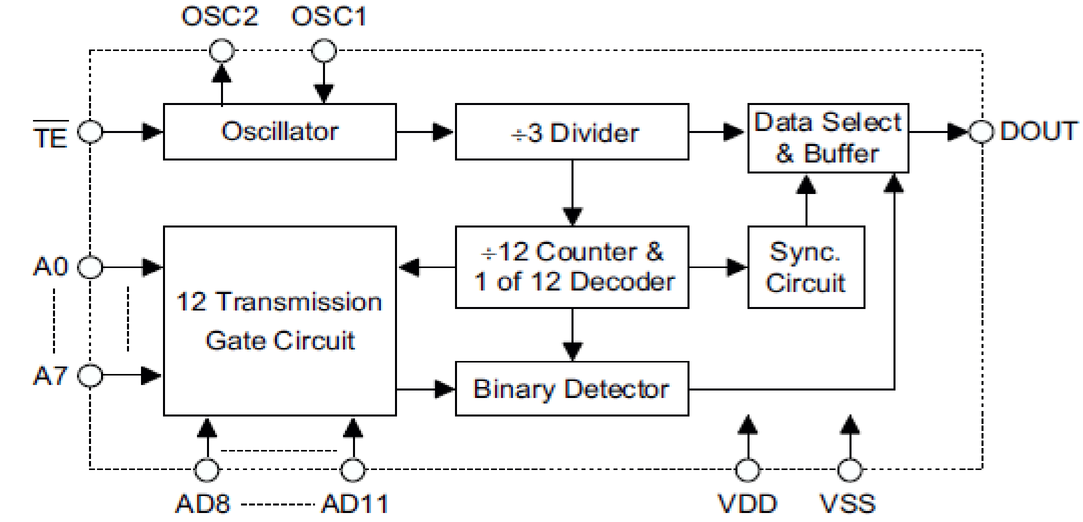
Function / Part No.	Address No.	Address/ Data No.	Data No.	Oscillator	Trigger	Package	Carrier Output	Negative Polarity
HT12A	8	0	4	455kHz resonator	D8~D11	18 DIP 20 SOP	38kHz	No
HT12E	8	4	0	RC oscillator	$\overline{TE}$	18 DIP 20 SOP	No	No

Note: Address/Data represents pins that can be address or data according to the decoders requirement.

D.4 Block Diagram

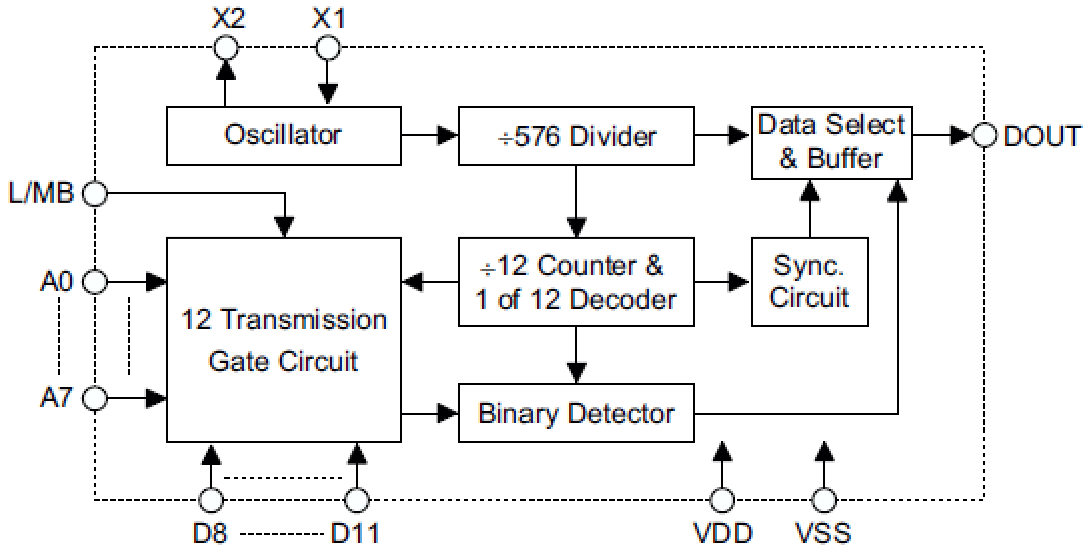
$\overline{TE}$ trigger

HT12E



DATA trigger

HT12A



Note: The address data pins are available in various combinations (refer to the address/data table).

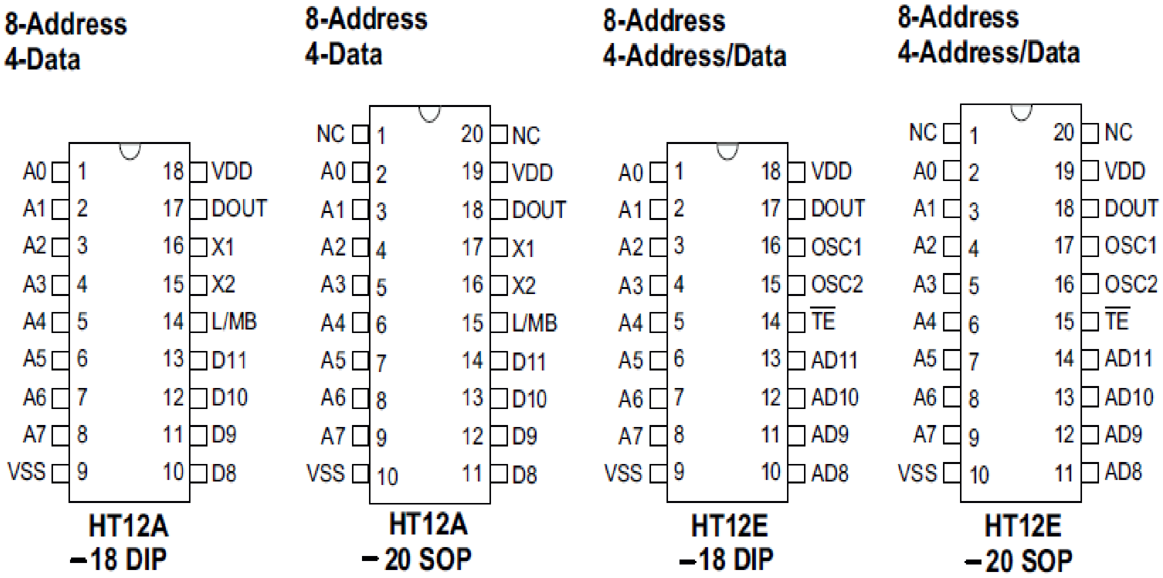


Figure D.1: Pin Assignment for HT12A/HT12E

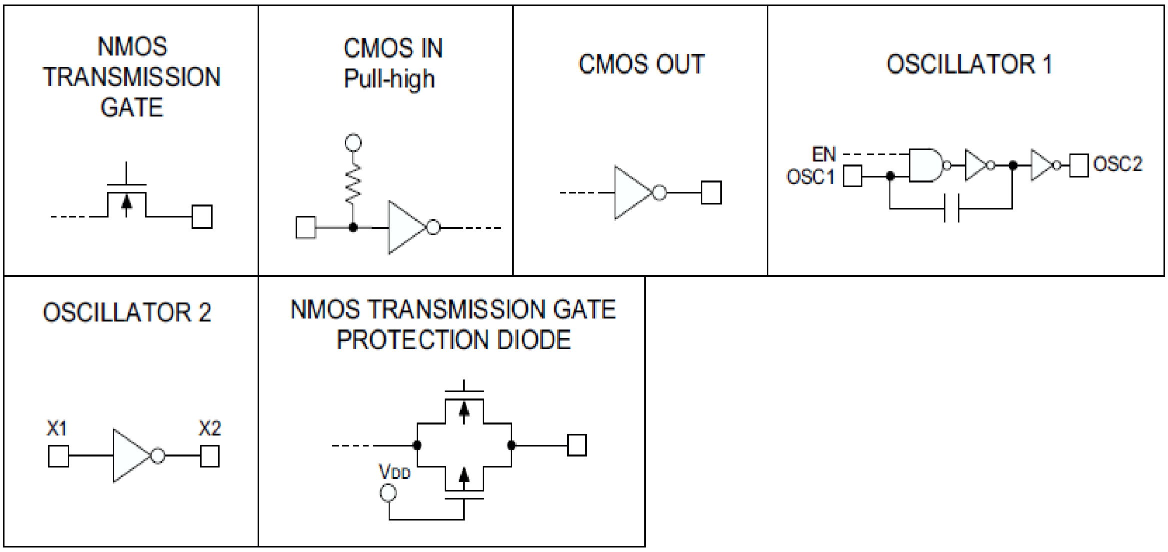
D.5 Pin Description

Pin Name	I/O	Internal Connection	Description
A0~A7	I	CMOS IN Pull-high (HT12A) NMOS TRANSMISSION GATE PROTECTION DIODE (HT12E)	Input pins for address A0~A7 setting These pins can be externally set to VSS or left open
AD8~AD11	I	NMOS TRANSMISSION GATE PROTECTION DIODE (HT12E)	Input pins for address/data AD8~AD11 setting These pins can be externally set to VSS or left open
D8~D11	I	CMOS IN Pull-high	Input pins for data D8~D11 setting and transmission enable, active low These pins should be externally set to VSS or left open (see Note)
DOUT	O	CMOS OUT	Encoder data serial transmission output
L/MB	I	CMOS IN Pull-high	Latch/Momentary transmission format selection pin: Latch: Floating or VDD Momentary: VSS

Pin Name	I/O	Internal Connection	Description
$\overline{\text{TE}}$	I	CMOS IN Pull-high	Transmission enable, active low (see Note)
OSC1	I	OSCILLATOR 1	Oscillator input pin
OSC2	O	OSCILLATOR 1	Oscillator output pin
X1	I	OSCILLATOR 2	455kHz resonator oscillator input
X2	O	OSCILLATOR 2	455kHz resonator oscillator output
VSS	I	—	Negative power supply, grounds
VDD	I	—	Positive power supply

Note: D8 ~ D11 are all data input and transmission enable pins of the HT12A. TE is a transmission enable pin of the HT12E.

D.6 Approximate internal connection



D.7 Absolute Maximum Ratings

Supply voltage (HT12A)..... -0.3v to 5.5v   Supply voltage (HT12E)..... -0.3v to 13v

Input voltage..... V_{SS} -0.3 to V_{DD} +0.3v   Storage Temperature..... -50˚C to 125˚C

Operating Temperature..... -20˚C to 75˚C

Note: These are stress ratings only. Stresses exceeding the range specified under 'Absolute Maximum Ratings' may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

Appendix E

2^{12} Series of Decoders Data Sheet

E.1 Features

- Operating voltage: 2.4V~12V
- Low power and high noise immunity CMOS technology
- Low standby current
- Capable of decoding 12 bits of information
- Binary address setting
- Received codes are checked 3 times
- Address/Data number combination
    - HT12D: 8 address bits and 4 data bits
    - HT12F: 12 address bits only
- Built-in oscillator needs only 5% resistor
- Valid transmission indicator
- Easy interface with an RF or an infrared transmission medium
- Minimal external components
- Pair with Holtek's 2^{12} series of encoders
- 18-pin DIP, 20-pin SOP package

E.2 Applications

- Burglar alarm system
- Smoke and fire alarm system
- Garage door controllers
- Car door controllers
- Car alarm system
- Security system
- Cordless telephones

- Other remote control systems

E.3 General Description

The 2^{12} decoders are a series of CMOS LSIs for remote control system applications. They are paired with Holtek's 2^{12} series of encoders (refer to the encoder/decoder cross reference table). For proper operation, a pair of encoder/decoder with the same number of addresses and data format should be chosen. The decoders receive serial addresses and data from a programmed 2^{12} series of encoders that are transmitted by a carrier using an RF or an IR transmission medium. They compare the serial input data three times continuously with their local addresses. If no error or unmatched codes are found, the input data codes are decoded and then transferred to the output pins. The VT pin also goes high to indicate a valid transmission. The 2^{12} series of decoders are capable of decoding informations that consist of N bits of address and 12-N bits of data. Of this series, the HT12D is arranged to provide 8 address bits and 4 data bits, and HT12F is used to decode 12 bits of address information.

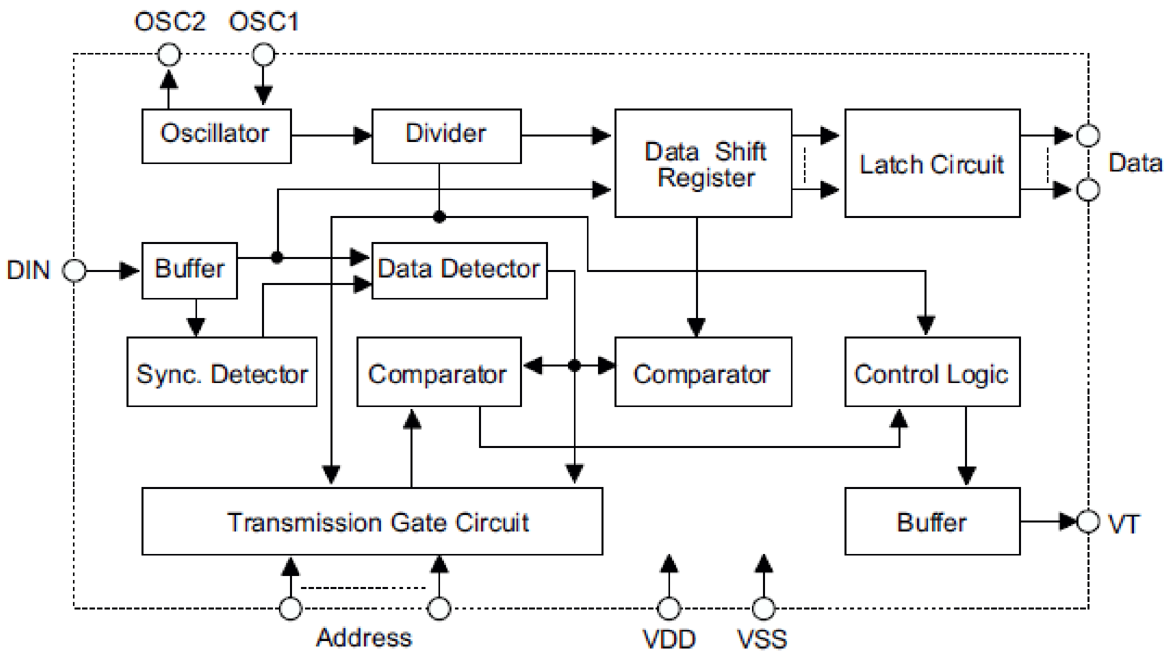
Table E.1: selection general description

Function / Part No.	Address No.	Data No.	Data Type	VT	Oscillator	Trigger	Package
HT12D	8	4	L	√	RC oscillator	DIN active "Hi"	18DIP, 20SOP
HT12F	12	0	—	√	RC oscillator	DIN active "Hi"	18DIP, 20SOP

Notes: Data type: L stands for latch type data output.

VT can be used as a momentary data output.

E.4 Block diagram



Note: The address/data pins are available in various combinations (see the address/data table).

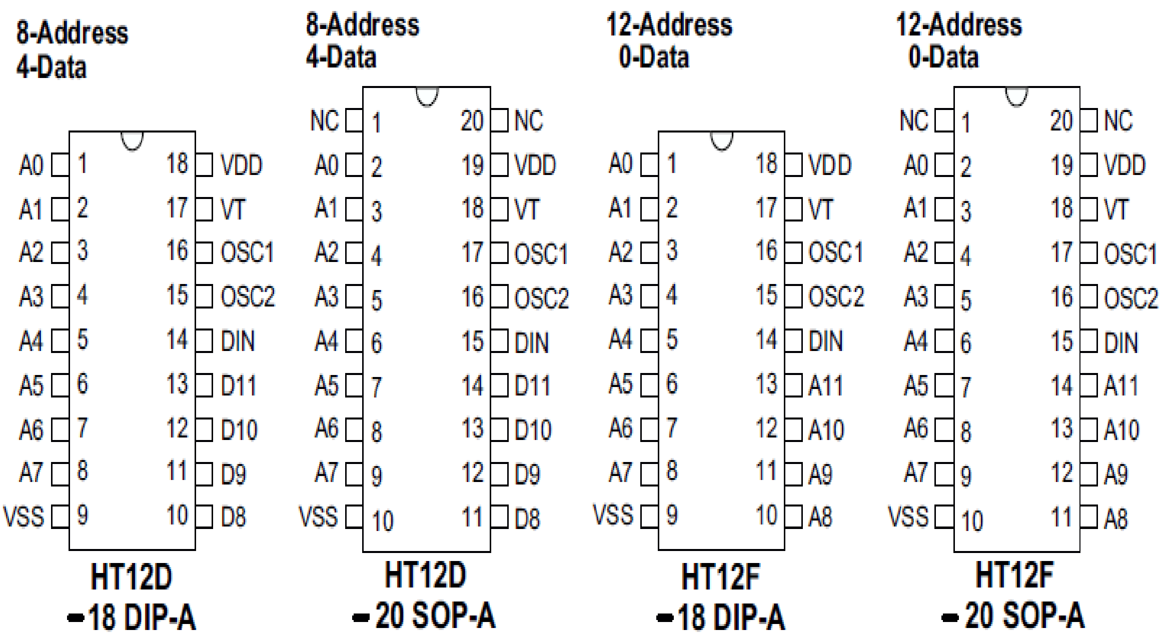
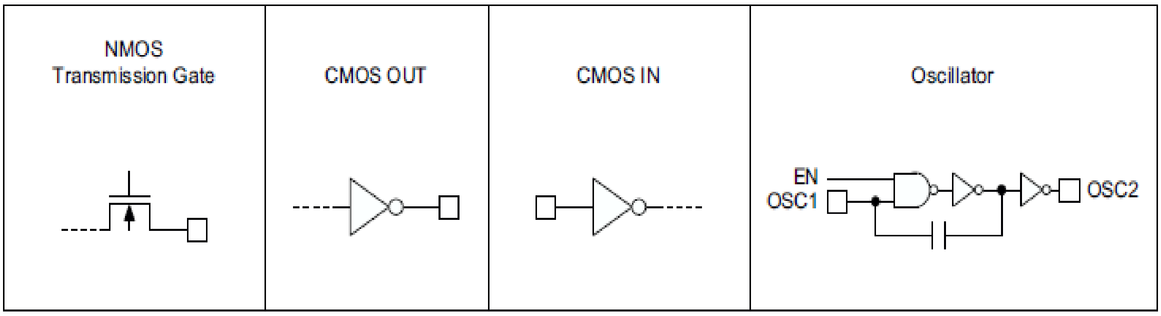


Figure E.1: Pin Assignment for HT12D/HT12F

E.5 Pin Description

Pin Name	I/O	Internal Connection	Description
A0~A11 (HT12F)	I	NMOS Transmission Gate	Input pins for address A0~A11 setting These pins can be externally set to VSS or left open.
A0~A7 (HT12D)			Input pins for address A0~A7 setting These pins can be externally set to VSS or left open.
D8~D11 (HT12D)	O	CMOS OUT	Output data pins, power-on state is low.
DIN	I	CMOS IN	Serial data input pin
VT	O	CMOS OUT	Valid transmission, active high
OSC1	I	Oscillator	Oscillator input pin
OSC2	O	Oscillator	Oscillator output pin
VSS	—	—	Negative power supply, ground
VDD	—	—	Positive power supply

E.6 Approximate internal connection circuits



E.7 Absolute Maximum Ratings

Supply Voltage ....- 0.3V to 13V Storage Temperature ....-50˚C to 125˚C

Input Voltage ....VSS-0.3 to VDD +0.3V Operating Temperature....-20˚C to 75˚C

Note: These are stress ratings only. Stresses exceeding the range specified under Absolute Maximum Ratings may cause substantial damage to the device. Functional operation of this device at other conditions beyond those Listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

E.8 Electrical Characteristics

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	2.4	5	12	V
I_{STB}	Standby Current	5V	Oscillator stops	—	0.1	1	μA
		12V		—	2	4	μA
I_{DD}	Operating Current	5V	No load, f_{OSC}=150kHz	—	200	400	μA
I_O	Data Output Source Current (D8~D11)	5V	V_{OH}=4.5V	–1	–1.6	—	mA
	Data Output Sink Current (D8~D11)	5V	V_{OL}=0.5V	1	1.6	—	mA
I_{VT}	VT Output Source Current	5V	V_{OH}=4.5V	–1	–1.6	—	mA
	VT Output Sink Current		V_{OL}=0.5V	1	1.6	—	mA
V_{IH}	"H" Input Voltage	5V	—	3.5	—	5	V
V_{IL}	"L" Input Voltage	5V	—	0	—	1	V
f_{OSC}	Oscillator Frequency	5V	R_{OSC}=51kΩ	—	150	—	kHz

Appendix F

ASK Super Regenerative Receiver Data Sheet

F.1 General Description

The ST-RX02-ASK is an ASK Hybrid receiver module.

A effective low cost solution for using at 315/433.92 MHZ.

The circuit shape of ST-RX02-ASK is L/C.

Receiver Frequency: 315 / 433.92 MHZ

Typical sensitivity: -105dBm

Supply Current: 3.5mA

IF Frequency: 1MHz

F.2 Features

- Low power consumption.
- Easy for application.
- Operation temperature range : － 20℃～＋70℃
- Operation voltage: 5 Volts.
- Available frequency at: 315/434 MHz

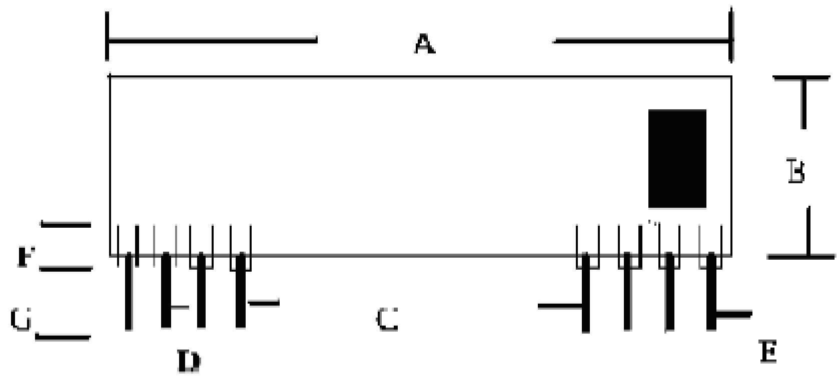
F.3 Applications

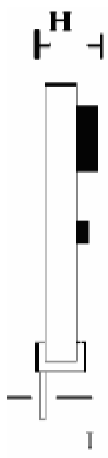
- Car security system
- Wireless security systems
- Sensor reporting
- Automation system
- Remote Keyless entry

F.4 Electrical Characteristics

CHARACTERISTIC	MIN	TYP	MAX	UNIT
Vcc Supply Voltage		5		VDC
Is Supply Current		3.5	4.5	mA
FR Receiver Frequency		315/434		MHz
RF Sensitivity(Vcc=5V 1Kbps Data Rate)		-105		dBm
Max Data Rate	300	1k	3k	Kbit/s
VOH High Level Output (I=30uA)	0.7Vcc			VDC
VOL Low Level Output (I=30uA)			0.3Vcc	VDC
Turn On Time(Vcc off-Turn on)		25		ms
TOP Operating Temperature Range	-20		70	℃
Output Duty	40		60	%

F.5 Mechanical Dimension





Dimensions	Millimeters	Dimensions	Millimeters
A	43.5 + 0.25mm	F	2.50 + 0.15mm
B	12 + 0.25mm	G	3.50 + 0.15mm
C	25.2 + 0.30mm	H	7.2 + (MAX)
D	2.54 + 0.05mm	I	0.32 + 0.05mm
E	0.65 + 0.05mm		

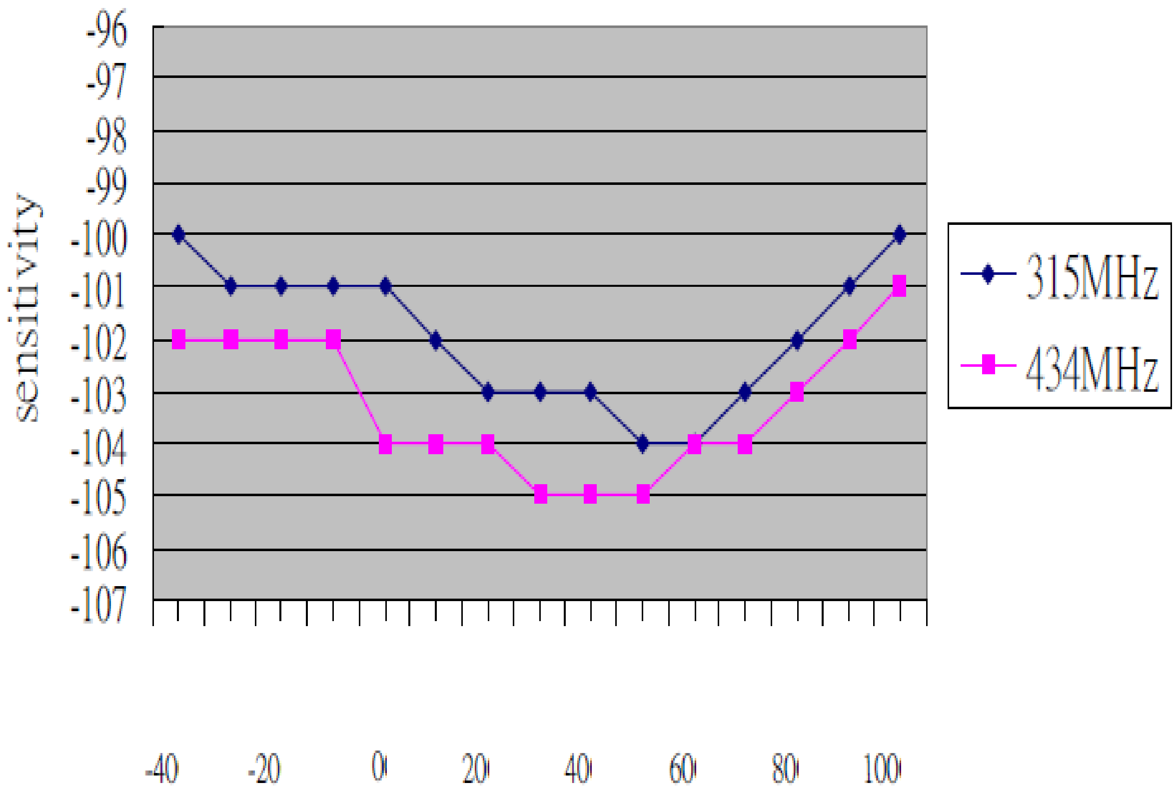
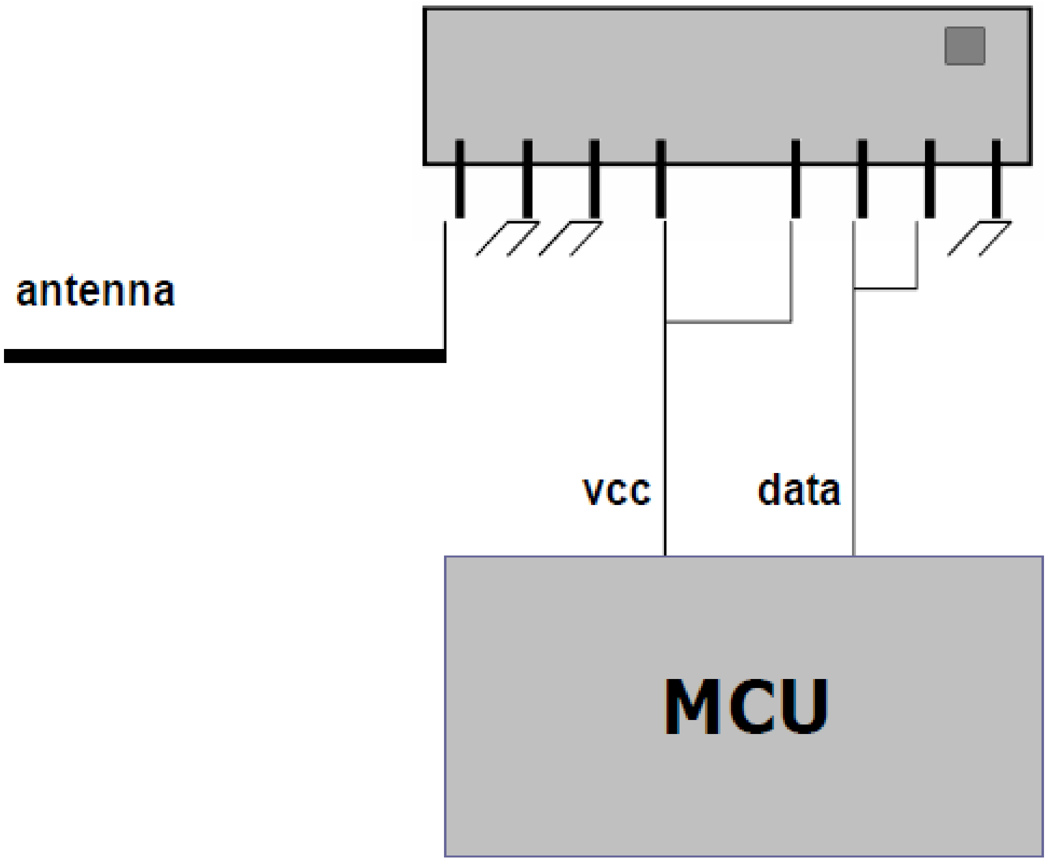


Figure F.1: Temperature VS sensibility

F.6 Typical Application



Remark: Antenna length about: 23cm for 315MHz 17cm for 434MHz

Appendix G

ASK Transmitter Module Data Sheet

G.1 General Description

The ST-TX01-ASK is an ASK Hybrid transmitter module.

ST-TX01-ASK is designed by the Saw Resonator, with an effective low cost, small size, and simple-to-use for designing.

Frequency Range:315 / 433.92 MHZ.

Supply Voltage: 3~12V.

Output Power: 4~16dBm

Circuit Shape: Saw

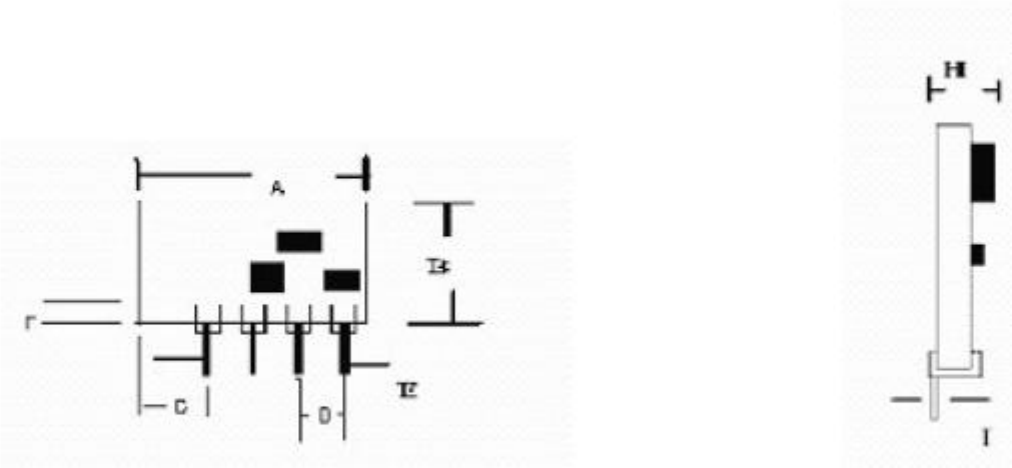
G.2 Applications

- Wireless security systems.
- Car Alarm systems.
- Remote controls.
- Sensor reporting.
- Automation system.

Table G.1: Absolute Maximum Ratings

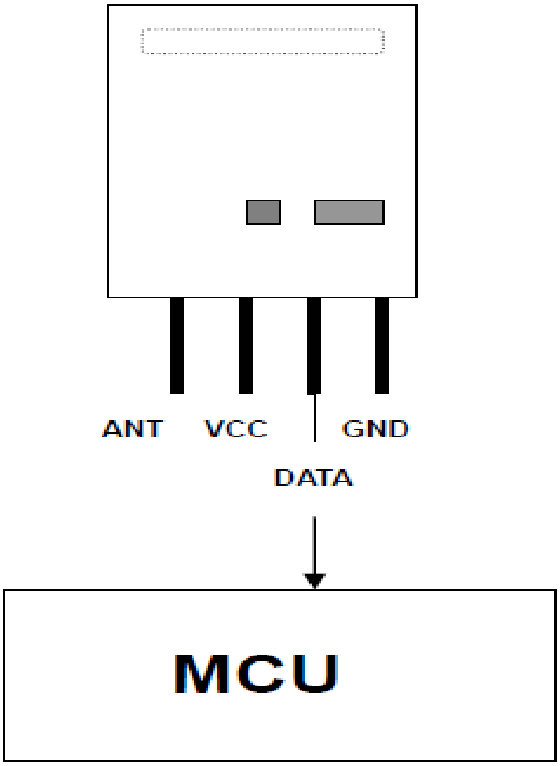
Parameter	Symbol	Condition		Specification					Unit
				Min.	Typical			Max.	
Operation Voltage					3V	5V	12V		V
Output power	Psens	DATA 5V 1Kbps Data Rate	315MHz		4	10	16		dBm
			Supply current		11	20	57		mA
			434MHz		4	10	16		dBm
			Supply current		11	22	59		mA
Tune on Time	Ton	Data start out by Vcc turn on		10		20			ms
Data Rate				200		1k		3k	bps
Input duty		Vcc=5V; 1kbps data rate		40				60	%
Temperature				-20				+80	℃

G.3 Pin Dimension



Dimensions	Millimeters	Dimensions	Millimeters
A	14+0.25mm	F	2.50+0.15mm
B	21+0.25mm	G	3.50+0.15mm
C	4.1+0.30mm	H	5.5mm
D	2.54+0.05mm	I	0.32+0.05mm
E	0.65+0.05mm		

G.4 Typical Application



Appendix H

ULN2803 and ULN2804 Data Sheet

Octal High Voltage, High Current Darlington

H.1 Transistor Arrays

The eight NPN Darlington connected transistors in this family of arrays are ideally suited for interfacing between low logic level digital circuitry (such as TTL, CMOS or PMOS/NMOS) and the higher current/voltage requirements of lamps, relays, printer hammers or other similar loads for a broad range of computer, industrial, and consumer applications. All devices feature open–collector outputs and freewheeling clamp diodes for transient suppression.

The ULN2803 is designed to be compatible with standard TTL families while the ULN2804 is optimized for 6 to 15 volt high level CMOS or PMOS.

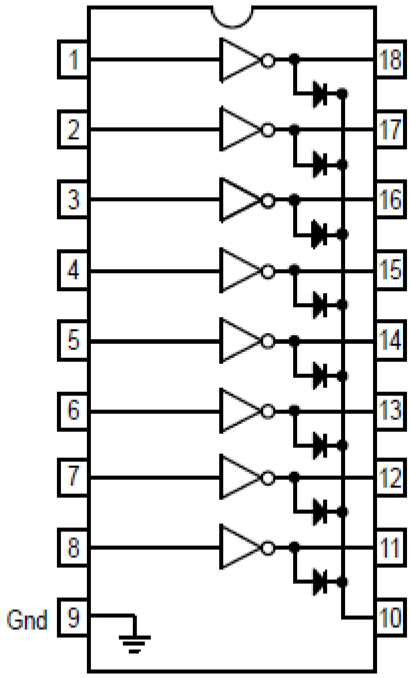


Figure H.1: Pin Connection

Maximum ratings (TA = 25°C and rating apply to any one device in the package, unless otherwise noted.)

Rating	Symbol	Value	Unit
Output Voltage	V_O	50	V
Input Voltage (Except ULN2801)	V_I	30	V
Collector Current – Continuous	I_C	500	mA
Base Current – Continuous	I_B	25	mA
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	–55 to +150	°C
Junction Temperature	T_J	125	°C

RqJA = 55°C/W Do not exceed maximum current limit per driver.

H.2 Ordering Information

Device	Characteristics		
	Input Compatibility	V_{CE}(Max)/I_C(Max)	Operating Temperature Range
ULN2803A ULN2804A	TTL, 5.0 V CMOS 6 to 15 V CMOS, PMOS	50 V/500 mA	T_A = 0 to + 70°C

H.3 ULN2803 ULN2804

Test figures

(See Figure Numbers in Electrical Characteristics Table)

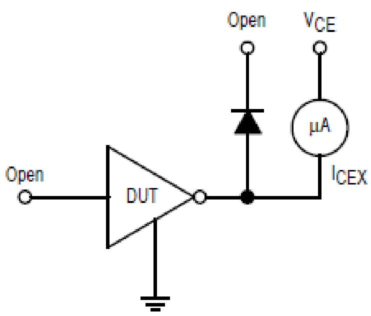


Figure H.1

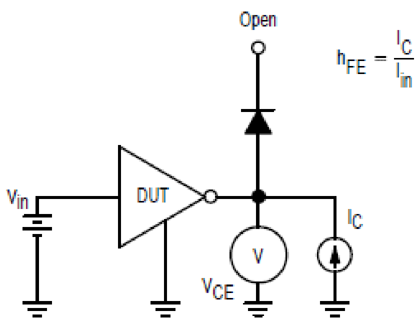


Figure H.2

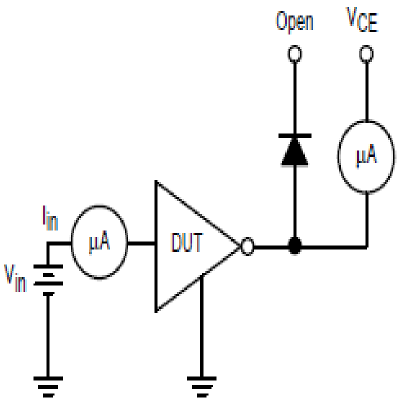


Figure H.3

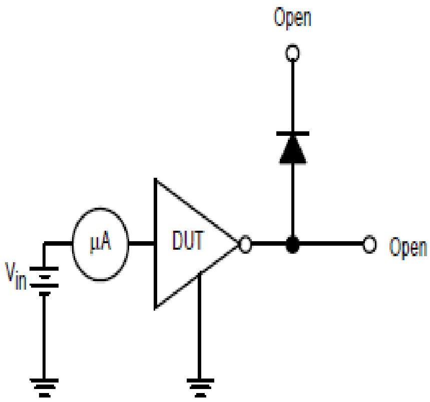


Figure H.4

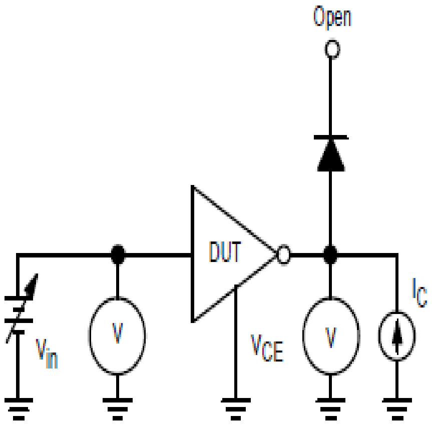


Figure H.5

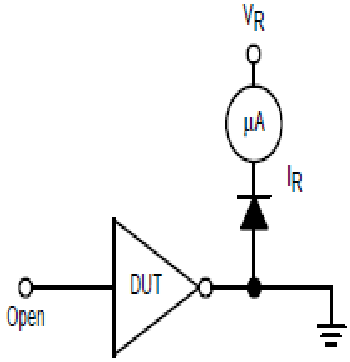


Figure H.6

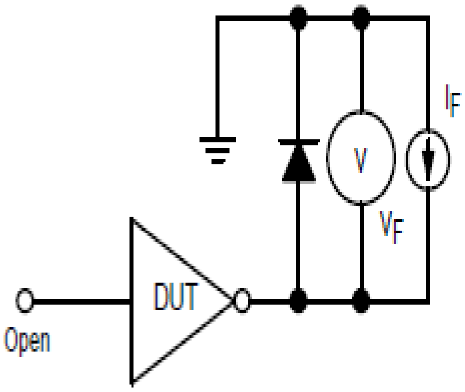


Figure H.7

Electrical characteristics (TA = 25°C, unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Output Leakage Current (Figure 1)		I_{CEX}				µA
(V_O = 50 V, T_A = +70°C)	All Types		–	–	100	
(V_O = 50 V, T_A = +25°C)	All Types		–	–	50	
(V_O = 50 V, T_A = +70°C, V_I = 6.0 V)	ULN2802		–	–	500	
(V_O = 50 V, T_A = +70°C, V_I = 1.0 V)	ULN2804		–	–	500	
Collector–Emitter Saturation Voltage (Figure 2)		$V_{CE(sat)}$				V
(I_C = 350 mA, I_B = 500 µA)	All Types		–	1.1	1.6	
(I_C = 200 mA, I_B = 350 µA)	All Types		–	0.95	1.3	
(I_C = 100 mA, I_B = 250 µA)	All Types		–	0.85	1.1	
Input Current – On Condition (Figure 4)		$I_{I(on)}$				mA
(V_I = 17 V)	ULN2802		–	0.82	1.25	
(V_I = 3.85 V)	ULN2803		–	0.93	1.35	
(V_I = 5.0 V)	ULN2804		–	0.35	0.5	
(V_I = 12 V)	ULN2804		–	1.0	1.45	
Input Voltage – On Condition (Figure 5)		$V_{I(on)}$				V
(V_{CE} = 2.0 V, I_C = 300 mA)	ULN2802		–	–	13	
(V_{CE} = 2.0 V, I_C = 200 mA)	ULN2803		–	–	2.4	
(V_{CE} = 2.0 V, I_C = 250 mA)	ULN2803		–	–	2.7	
(V_{CE} = 2.0 V, I_C = 300 mA)	ULN2803		–	–	3.0	
(V_{CE} = 2.0 V, I_C = 125 mA)	ULN2804		–	–	5.0	
(V_{CE} = 2.0 V, I_C = 200 mA)	ULN2804		–	–	6.0	
(V_{CE} = 2.0 V, I_C = 275 mA)	ULN2804		–	–	7.0	
(V_{CE} = 2.0 V, I_C = 350 mA)	ULN2804		–	–	8.0	
Input Current – Off Condition (Figure 3) (I_C = 500 µA, T_A = +70°C)	All Types	$I_{I(off)}$	50	100	–	µA
DC Current Gain (Figure 2) (V_{CE} = 2.0 V, I_C = 350 mA)	ULN2801	h_{FE}	1000	–	–	–
Input Capacitance		C_I	–	15	25	pF
Turn–On Delay Time (50% E_I to 50% E_O)		t_{on}	–	0.25	1.0	µs
Turn–Off Delay Time (50% E_I to 50% E_O)		t_{off}	–	0.25	1.0	µs
Clamp Diode Leakage Current (Figure 6) (V_R = 50 V)	T_A = +25°C	I_R	–	–	50	µA
	T_A = +70°C				100	
Clamp Diode Forward Voltage (Figure 7) (I_F = 350 mA)		V_F	–	1.5	2.0	V

Output Characteristics

Typical characteristic curves - TA = 25°C, unless otherwise noted

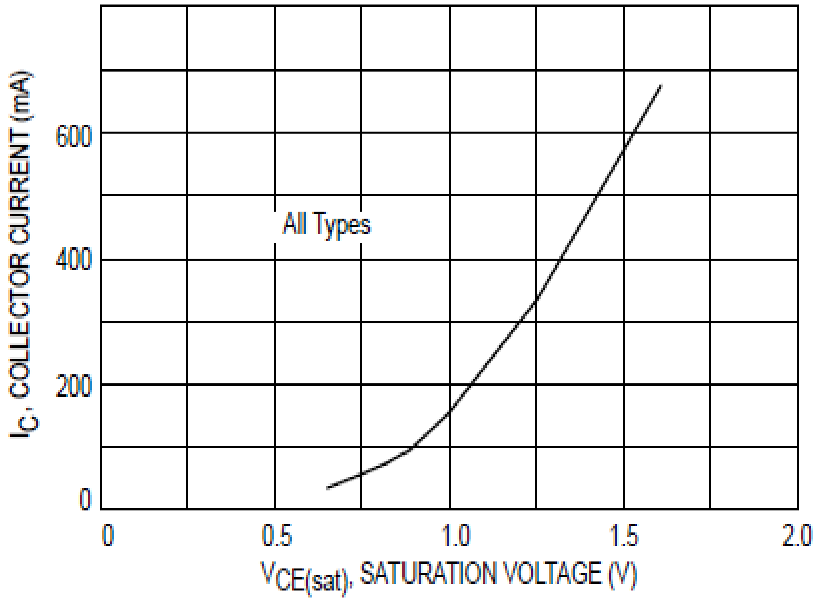


Figure H.8: Output Current versus Saturation Voltage

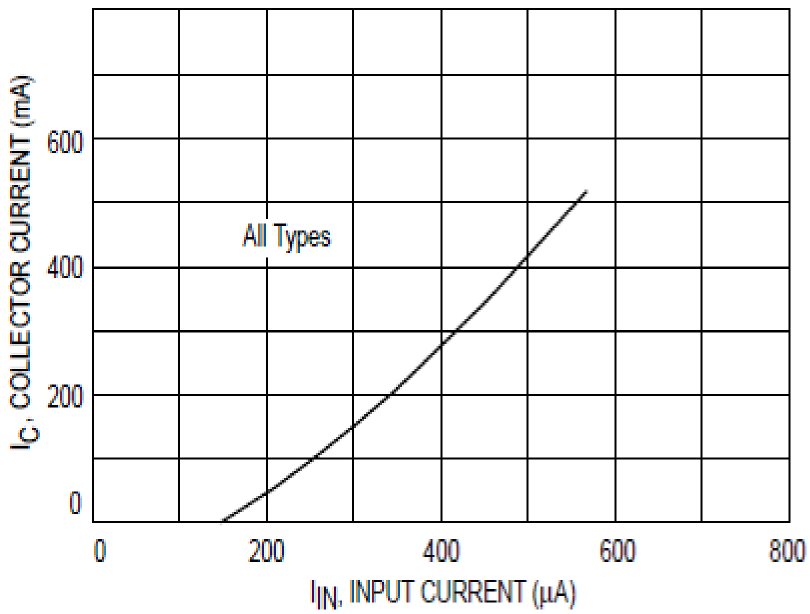


Figure H.9: Output Current versus Input Current

Input Characteristics

Typical characteristic curves - TA = 25°C, unless otherwise noted

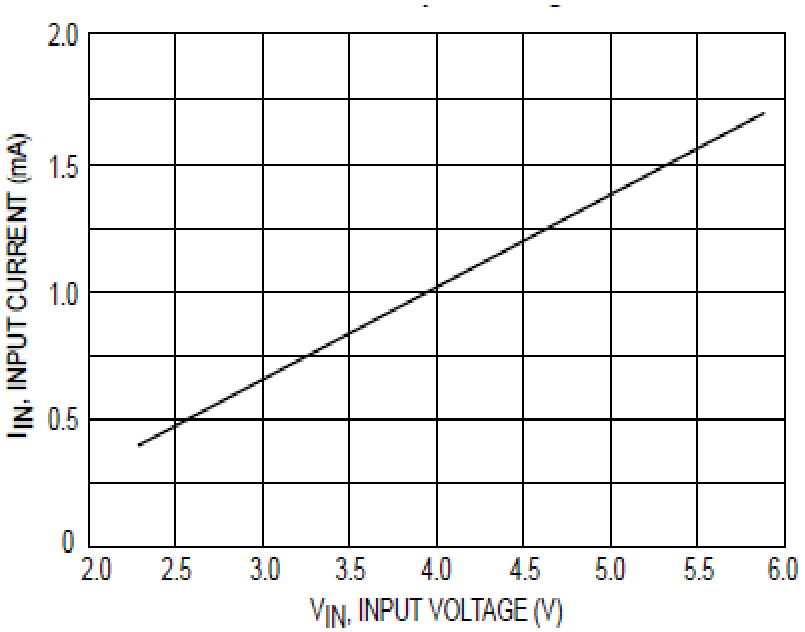


Figure H.10: ULN2803 Input Current versus Input Voltage

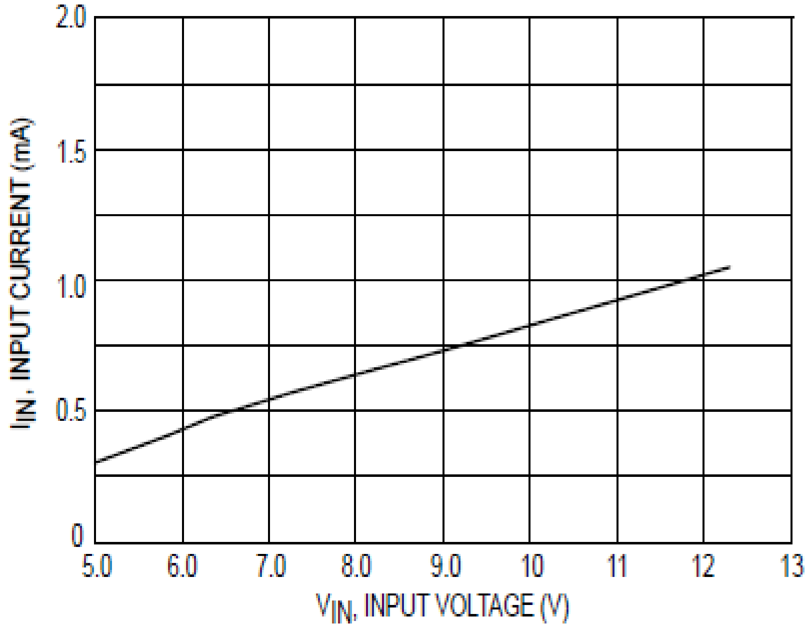


Figure H.11: ULN2804 Input Current versus Input Voltage

Appendix I

Positive Voltage Regulator Data Sheet

3- Terminal 1A Positive Voltage Regulator

I.1 Features

- Output Current up to 1A.
- Output Voltage: 5, 6, 8, 9, 10, 12, 15, 18, 24v.
- Terminal Overload Protection.
- Short – Circuit Protection.
- Output Transistor Safe Operation Area Protection.

I.2 Description

The LM78XX series of three – terminal positive regulator is available in the TO-220 package and with several fixed output voltage, making them useful in a wide range of applications. Each type employs internal current limiting, thermal shut – down, and safe operating area protection. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed – voltage regulators, these devices can be used with external components for adjustable voltages and currents.

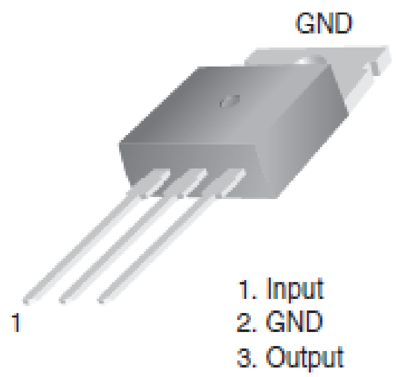


Figure I.1: Voltage Regulator

Table I.1: ordering Information

Product Number	Output Voltage Tolerance	Package	Operating Temperature	Packing Method
LM7805CT				
LM7806CT				
LM7808CT				
LM7809CT				
LM7810CT	±4%		-40°C to +125°C	
LM7812CT				
LM7815CT		TO-220 (Single Gauge)		
LM7818CT				Rail
LM7824CT				
LM7805ACT				
LM7809ACT				
LM7810ACT	±2%		0°C to +125°C	
LM7812ACT				
LM7815ACT				

Note: above output voltage tolerance is available at 25˚C.

I.3 Block Diagram

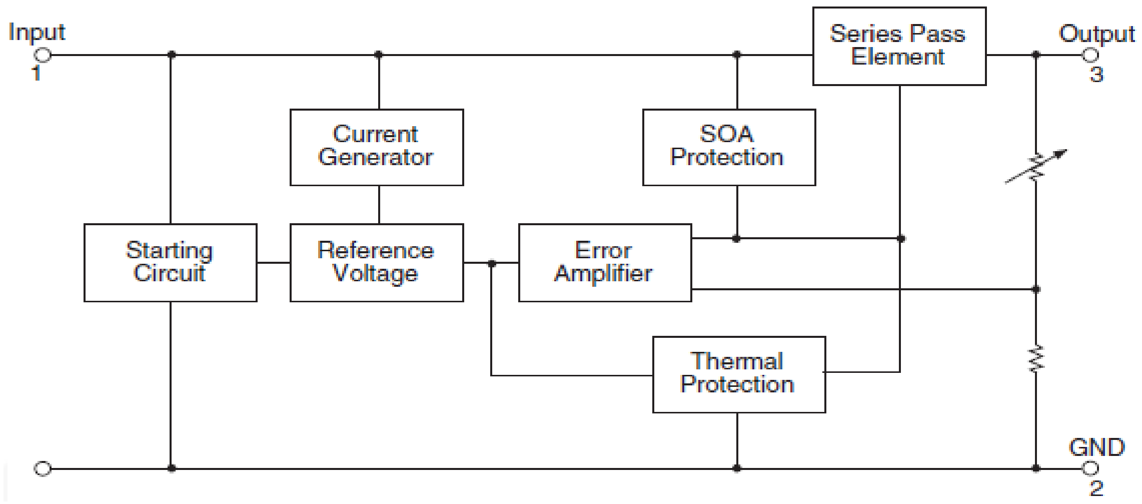


Figure I.2: Block Diagram

I.4 Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device.

The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions my affect device reliability. The absolute maximum ratings are stress ratings only. Values are at T_A = 25˚C unless otherwise noted.

Symbol	Parameter		Value	Unit
V_I	Input Voltage	V_O = 5 V to 18 V	35	V
		V_O = 24 V	40	
$R_{\theta JC}$	Thermal Resistance, Junction-Case (TO-220)		5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-Air (TO-220)		65	°C/W
T_{OPR}	Operating Temperature Range	LM78xx	-40 to +125	°C
		LM78xxA	0 to +125	
T_{STG}	Storage Temperature Range		- 65 to +150	°C

Electrical Characteristics (LM7805)

Refer to the test circuit, -40˚C < T_J < 125˚C, I_O = 500 mA, V_I = 10v, C_I = 0.1μF, unless other wise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_O	Output Voltage	T_J = +25°C		4.80	5.00	5.20	V
		I_O = 5 mA to 1 A, $P_O \leq$ 15 W, V_I = 7 V to 20 V		4.75	5.00	5.25	
Regline	Line Regulation(2)	T_J = +25°C	V_I = 7 V to 25 V		4.0	100.0	mV
			V_I = 8 V to 12 V		1.6	50.0	
Regload	Load Regulation(2)	T_J = +25°C	I_O = 5 mA to 1.5 A		9.0	100.0	mV
			I_O = 250 mA to 750 mA		4.0	50.0	
I_Q	Quiescent Current	T_J = +25°C			5	8	mA
ΔI_Q	Quiescent Current Change	I_O = 5 mA to 1 A			0.03	0.50	mA
		V_I = 7 V to 25 V			0.30	1.30	
$\Delta V_O/\Delta T$	Output Voltage Drift(3)	I_O = 5 mA			-0.8		mV/°C
V_N	Output Noise Voltage	f = 10 Hz to 100 kHz, T_A = +25°C			42		μV
RR	Ripple Rejection(3)	f = 120 Hz, V_I = 8 V to 18 V		62	73		dB
V_{DROP}	Dropout Voltage	T_J = +25°C, I_O = 1 A			2		V
R_O	Output Resistance(3)	f = 1 kHz			15		mΩ
I_{SC}	Short-Circuit Current	T_J = +25°C, V_I = 35 V			230		mA
I_{PK}	Peak Current(3)	T_J = +25°C			2.2		A

Notes: - Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

- These parameters, although guaranteed, are not 100% tested in production.