Chapter Five

Conclusions and Recommendation

5.1 Conclusion:

This thesis has presented a power estimation for a simplified AMBA bus chip architecture with a focus on a system level analysis using matlab, the system power estimation model was segmented to a five power models.

Part of the power estimation model was dedicated to estimate power in the input stage by making it work at high activity level transmitting data to the output device and managing all the device connected, the reached result recovered that most of the power was consumed in this device at about 60 percent of the total power

Another part of the power estimation model was dedicated to the output stage dealing with it as a slave device only receiving and transmitting data with input stage the reached result showed that only 10 percent of the power was consumed in this stage.

There was a model dedicated to the bus wires which is the most focused part on this thesis by making the power estimation depends on the system activity by using two wire power estimation for high system activity and normal system activity, the high system activity was proposed as a high power level model, the normal system activity was proposed as an power estimation for an modified RLC network, the reached result in both models shows that the least power dissipation was in the bus wire at less than 1 percent of the total power.

The other two power estimation model was dedicated to the middle stage devices (decoder and arbiter), those two devices works only to help the input device to communicate with the output device and vice versa, the reached power result shows that only about 31 percent of the total power was consumed in those devices.

5.2 Recommendation:

This thesis presented only power estimation for an a SoC chip, a future direction can be a reduction techniques for high level synthesis based design frameworks enabling clock-gating from ANSI C description, This approach can be extended for some of the dynamic and static power reduction techniques such as operand-isolation, sequential clock-gating, power-gating. This will help in reducing the power consumption of design using multiple techniques while remaining at high-level.

Formalization of the high-level synthesis framework help to control and get a better view of how design will look like, Existing frameworks require manual refinements on the functional model of the target design. These manual refinements are applied to convert the pure sequential code into a structural code, which contains the information of the macro architecture of the design. In the macro-architecture, generally designers aim to include necessary parallelism using threads to explicitly bring out the concurrency opportunities in the sequential code. During the conversion process various minute details are inserted in the design description, which includes pipelining stages to achieve the desired throughput or necessary parallelism needed to meet the performance requirement.