Chapter Four

Results and Discussion

4.1 Introduction:

This chapter shows the simulation result attained by describing the power consumed in the SoC and also shows the simulation parameter and makes a full system power consumption comparison in all the system level.

4.2 Simulation Design and Model:

The simulation was done in Matlab R2013a, a modified ARM AMBA was introduced as the main platform for the simulation, and the power model was divided to five segments as shown earlier, the control signal was proposed for worst case scenario (high system activity).

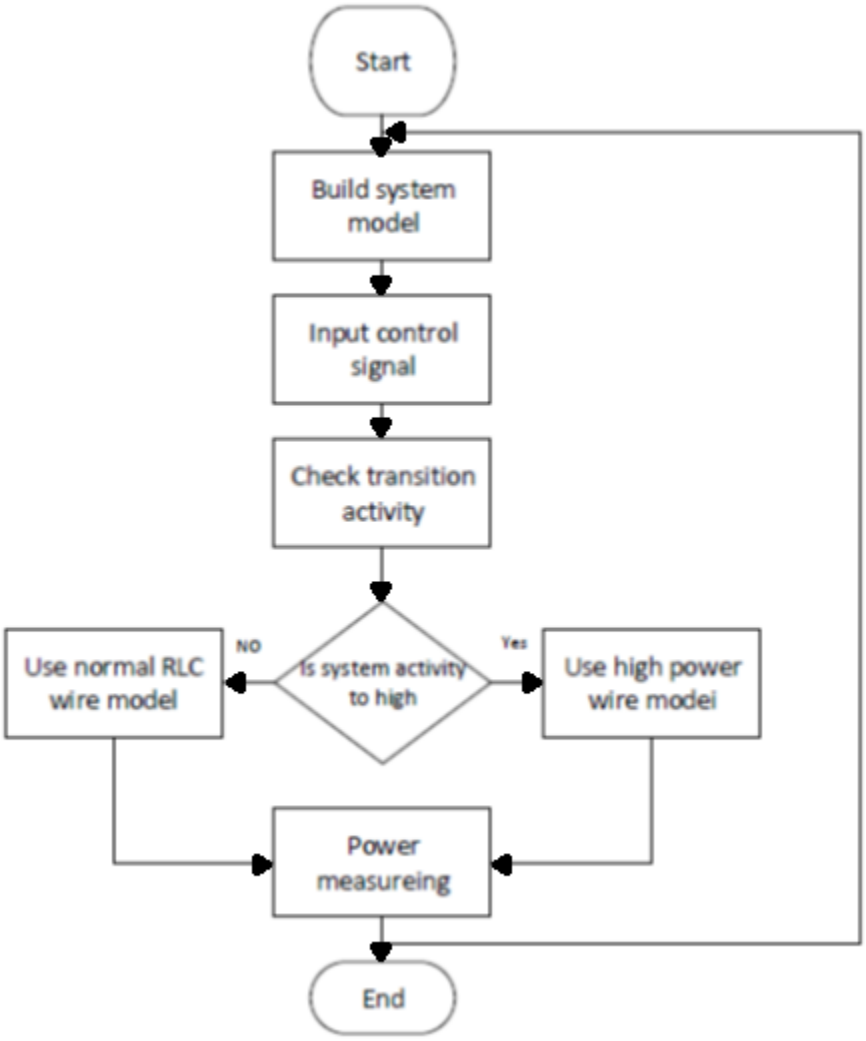

Figure 4.1: Power estimation simulation flow.

4.3 Simulation Parameters:

We considered in this thesis some simulation parameter as shown below in table 4.1.

Table 4.1: System parameter

Clock frequency (f)	1.68GHz
Operational voltage (Vdd)	1.1V
Sample number (M)	50 sample
Resistance of wire	98.2 KΩ/m
Coupling reactance of wire ($x_{inter)}$	136.671KΩ/m
Self-reactance of wire ($x_{line)}$	19.04 KΩ/m
Number of master device	1
Number of slave device	1

4.4 Simulation Result:

4.4.1 Power Estimation in the Input Stage:

The power estimated in figure 4.2 resembles the power consumed in the master device, the master device are proposed to be active for the entire simulation period communicating and sending data to the slave device.

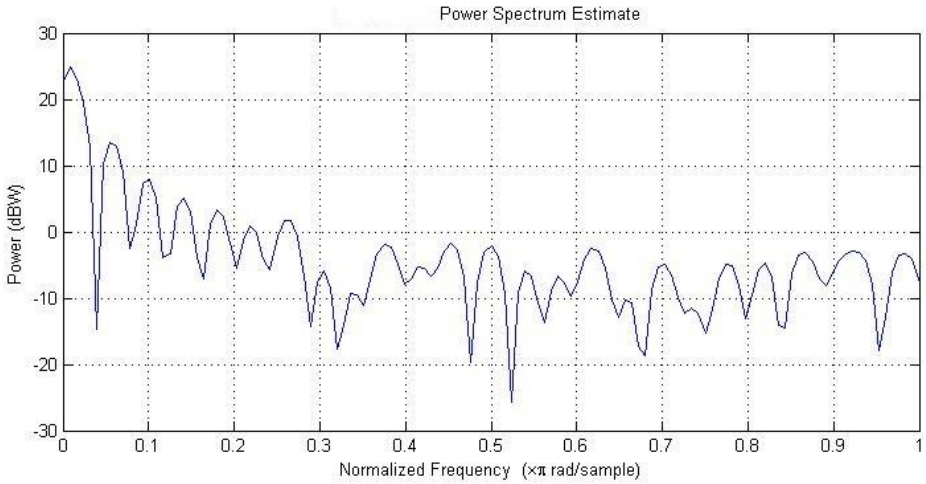

Figure 4.2: Power estimated in the input stage

4.4.2 Power Estimated in the Decoder:

The power estimated in figure 4.3 resembles the power consumed in the decoder, decoder activity is low compared to the master device because it's only active when the master needs to select the slave device and when some multiplexing is needed by the slave device.

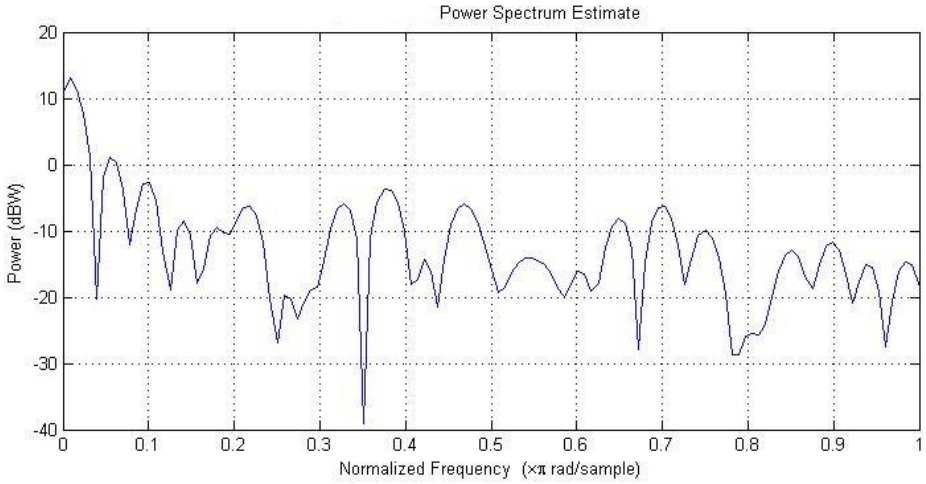

Figure 4.3: Power estimated in the decoder

4.4.3 Power Estimated in the Arbiter:

The power estimated in figure 4.4 resembles the power consumed in the arbiter, the arbitration process depends on the master devices activity hence the arbiter job is to be sure that only one master can use the bus in any time by using an arbitration scheme.

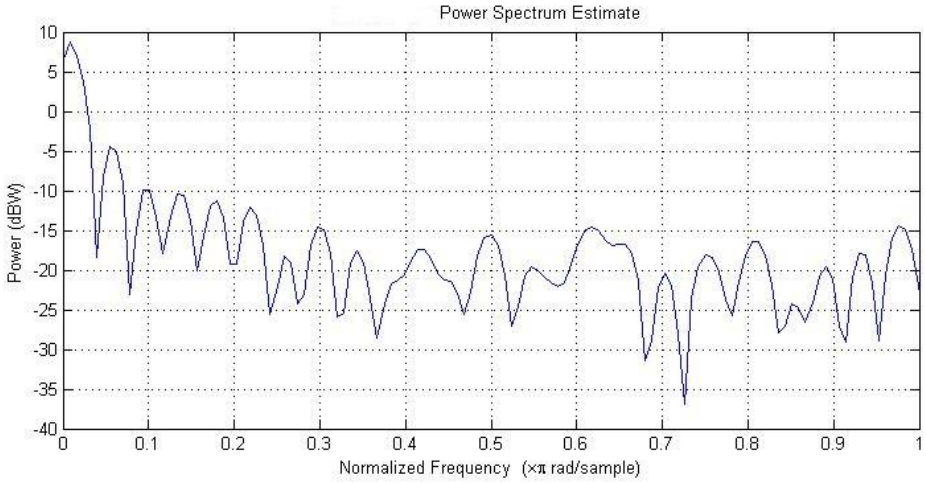

Figure 4.4: Power estimated in the arbiter

4.4.4 Power Estimated in the Wires:

Power dissipated in the wires was estimated by using two power system model, the first model is developed for high frequency response system with low system activity, dealing with the wire as an RLC network the power estimation for this model is shown in figure 4.5(a), the second model was developed for high frequency response system with high system activity, depending on the transition activity between wire interconnect and the power consumed in the repeater and the vias, power estimation for the second model is shown in figure 4.5(b).

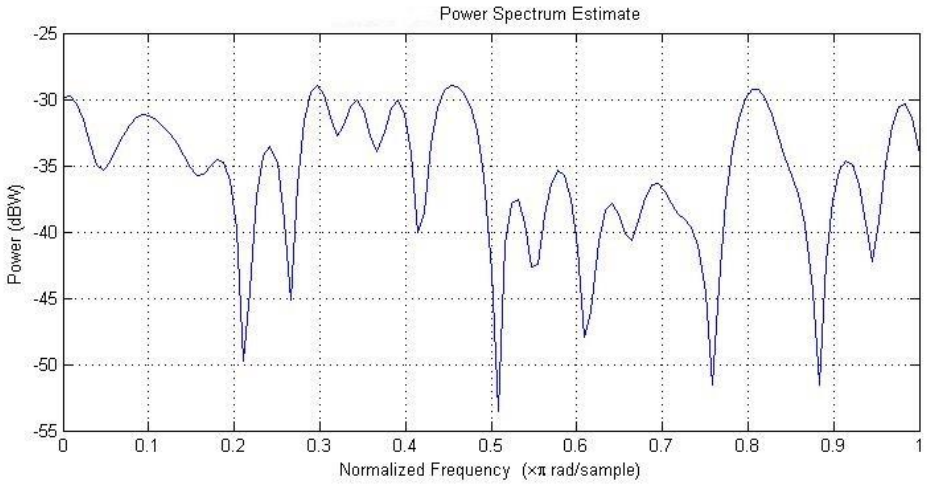

Figure 4.5(a): Power estimated in the wire for normal high frequency system

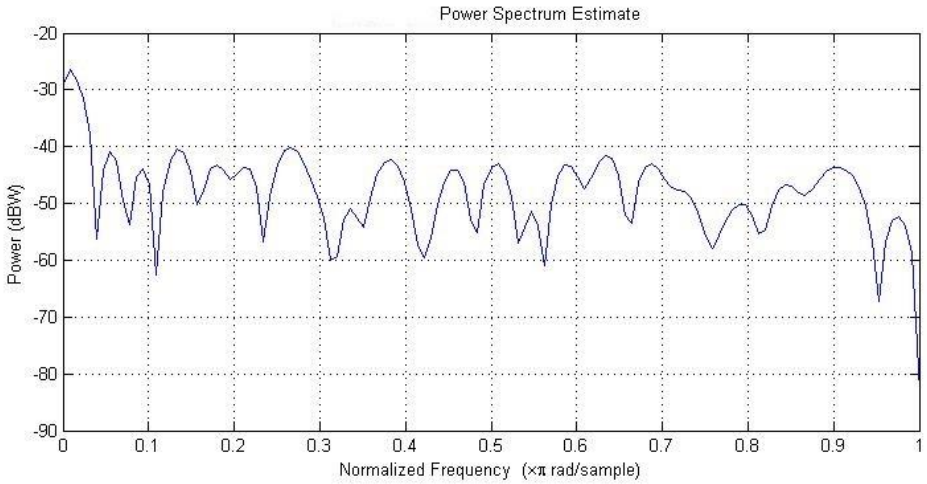

Figure 4.5(b): Power estimated in the wire for high system activity

4.4.5 Power Estimated in the Output Stage:

The power estimated in figure 4.6 resembles the power consumed in the slave device, meaning that the power consumed depends only on the slave device activity sending and receiving data to and from the master device.

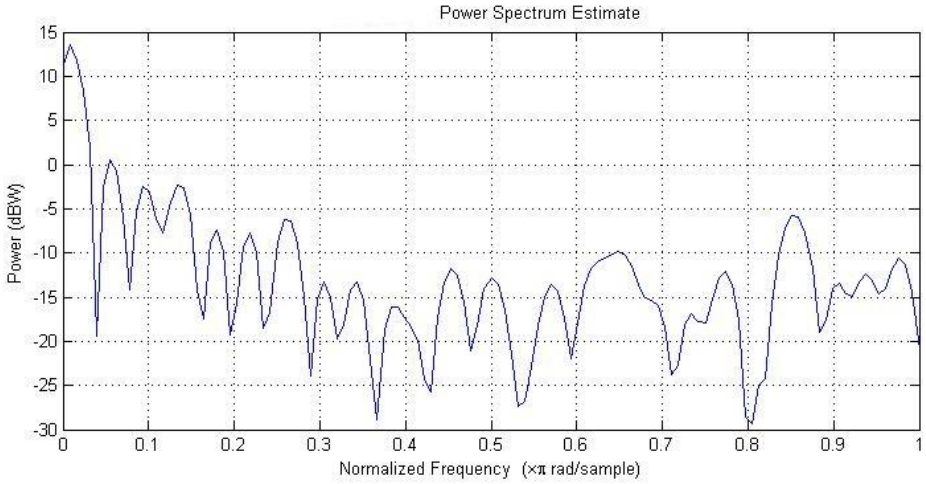

Figure 4.6: Power estimated in the output stage

4.4.6 Power Comparison for System Components:

By reviewing the result in figures 4.7 it can be seen that the major power consumption was in the input stage (master device) as about 58% of the total power dissipation, which can be related to the high activity for the master device in initiating data transmission and managing all the connected devices, in the other hand the least power consumption was in the bus wires at less than 1% of the total dissipated power, that's because the dissipated power only depends on bus wire material, length and wire interconnects, the other devices consumed power is about the same at 14% of total power consumed in the decoder and 17% on the output stage and 10% in the arbiter, which can be related to their work nature as they are active for bursts of time when they are communicating with the master device, other the less they are idle.

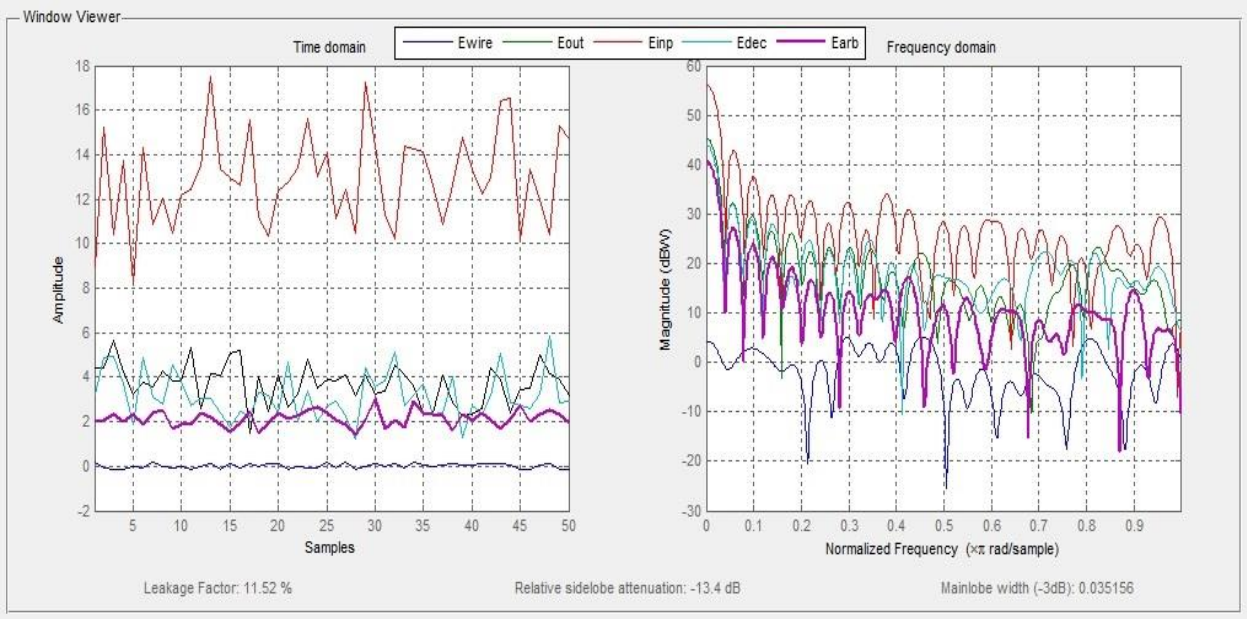

Figure 4.7(a): Power values compared for all system components

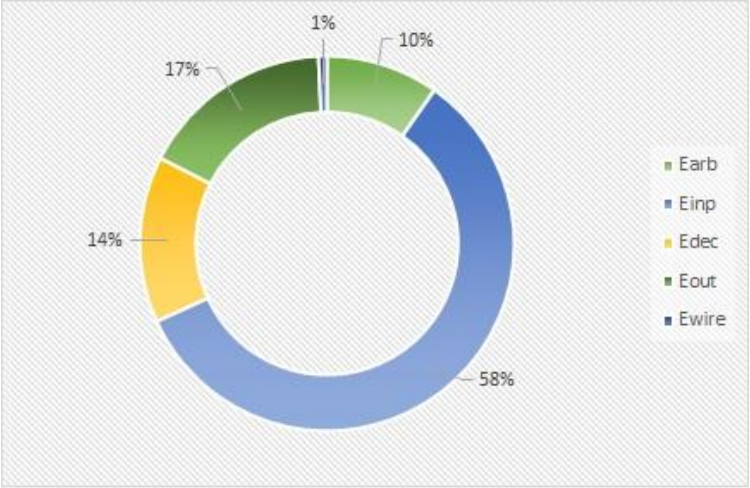

Figure 4.7(b): Power consumption percentage for all system components

4.5 Compare Result to Other Work:

Comparing the attained result to the result presented by K.Lahiri and A.Raghnathan[29] we can see in their work that the least power consumption part of the On-Chip Communication system is in the bus line then the logic devices and lastly in the master and slave devices which

can be seen as nearly similar to the result presented in this work, Figure 4.8 shows one of their result.

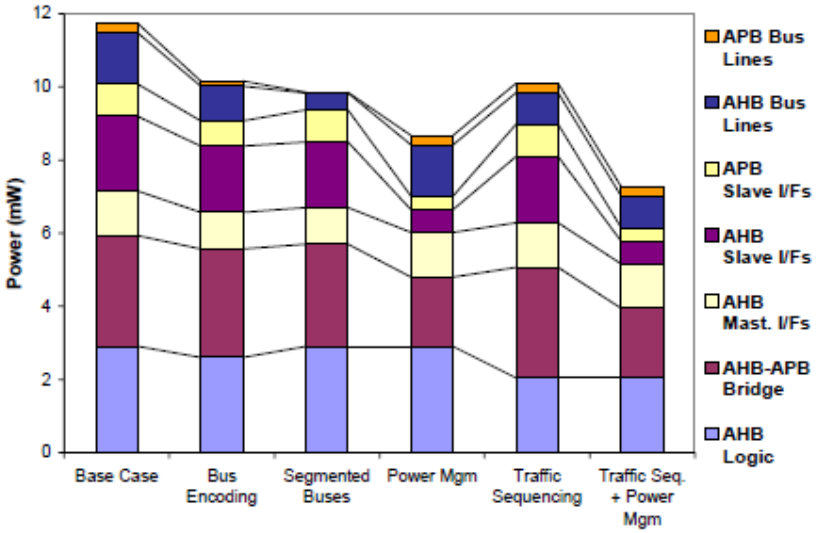

Figure 4.8: Power comparison inside the chip, source: K.Lahiri and A.Raghnathan[29]

4.6 Chapter Summary:

This chapter is introducing the results attained by the implemented simulation which describe the power consumed and dissipated in all the on-chip communication system level, divided into the power consumed in the bus wire and logic devices and the master and slave devices, giving system parts power consumption comparison and a brief comparison to a similar work.