

**Chapter One**  
**Introduction**

## 1.1 Introduction:

Managing power consumption in complex System-on-Chips (SoCs) and custom processors is emerging as the biggest concern for designers. These SoCs and processors are vital parts of embedded systems used in electronic equipment's ranging from laptop computers, mobile phones to personal digital assistants (PDA), etc. Quality/Performance of such devices is not only measured by what kind of functionalities these devices are capable of performing, but also how long these gadgets survive without plugging into power outlets for recharging. There is an increased demand for reduced form factor or lower size of such devices, which is generally determined by the size of the battery used to run these devices. Another need for controlling power consumption of the design is to decrease power density of devices on a single die. A report shows that power density of some designs can reach the power density of a rocket nozzle in future, if power aware design approaches are not used. The reasons cited above have motivated engineers to look into power aware design methodologies.

Traditionally the hardware design flow begins from the register transfer level (RTL) whereas the design is synthesized to the gate-level, and after further processing at the lower abstraction levels a chip is manufactured. Methodologies for power estimation and optimization at the RTL or lower-level are well studied. In the recent past, modeling at higher level of abstraction was advocated for quick turnaround. Increased demand and reduced time-to-market requirements for electronic equipment's have forced designers to adopt high-level modeling in their design-flow. Design methodologies, where reduction of power consumption of such systems can be done at the high-level, have become the need of the hour. We know that any optimization requires good analysis of the design; and so is the case with managing the power consumption of the design. To reduce the power consumption in the final product, it is necessary to have an estimate of the power consumption early on. It is becoming essential to utilize design methodologies to reduce and estimate power consumption at the high-level.

## 1.2 Problem Statement:

Increasing System-on-Chip (SoC) complexity, coupled with poor scaling trends of global interconnect, are together making on-chip communication a bottleneck to improving overall system performance and power consumption. As a result of this trend, recent research has focused on analyzing and optimizing the power consumed by global interconnect wires, which represent

one part of the on-chip communication architecture, Power estimation for any SoC system must be measured for real work environment to give an accurate result, in many native works the power estimation are approached from a general point of view or by including one real workload factor as including global wire RLC as in R. Kar [1], or combining two or more methods to have more accurate estimation as in by Ghodrat. And by Marcello Lajolo [2].

### **1.3 Proposed Solution:**

By presenting a systematic evaluation and analysis of the power consumed by a state-of-the-art communication architecture (the AMBA on chip bus), using a commercial design flow. We focus on developing a quantitative understanding of the relative contributions of different communication architecture components to its power consumption, and the factors on which they depend. We decompose the communication architecture power into power consumed by logic components (such as arbiters, decoders, bus bridges), global bus lines (that carry address, data, and control information), and bus interfaces. We also perform studies that analyze the impact of varying application traffic characteristics, and varying SoC complexity, on communication architecture power This approach will provide more accurate power estimation by developing a model that include high power and high frequency effects.

### **1.4 Literature Review:-**

Low-power design techniques has mostly focused on estimating and optimizing power consumption in the individual system-on-chip components (application-specific hardware, embedded software, memory hierarchy, buses, etc.) separately. Various power estimation and minimization techniques for hardware at the transistor, logic, architecture, and algorithm levels have been developed in the recent years, and are summarized in [3, 4, 5 and 6]. Power analysis techniques have been proposed for embedded software based on instruction-level characterization [7] and simulation of the underlying hardware [8]. Power estimation and optimization techniques for other system-on-chip components, including memory hierarchies and system buses, have been proposed, and in [9, 10].

Recently, researchers have started investigating system-level tradeoffs and optimizations whose effects transcend the individual component boundaries. Techniques for synthesis of multiprocessor system architectures and heterogeneous distributed HW/SW architectures for real-

time specifications were presented in [11, 12]. These approaches either assume that all tasks are pre-characterized with respect to all possible implementations for delay and power consumption, or assume a significantly simplified power dissipation model. In [13] and [14], separate execution of an instruction set simulator (ISS) based software power estimator, and a gate-level hardware power estimator were used to drive exploration of tradeoffs in an embedded processor with memory hierarchy, and to study HW/SW partitioning tradeoffs. The traces for the ISS and hardware power estimator were obtained from timing-independent system level behavioral simulation.

### 1.5 Methodology:-

The power estimation methodology used in this work is illustrated in Figure 1.1, Architectural configuration parameters of the AMBA bus was taken approximated to a microprocessor chip, By calculating system power consumed in any level using high power high frequency model we will have an accurate estimation.

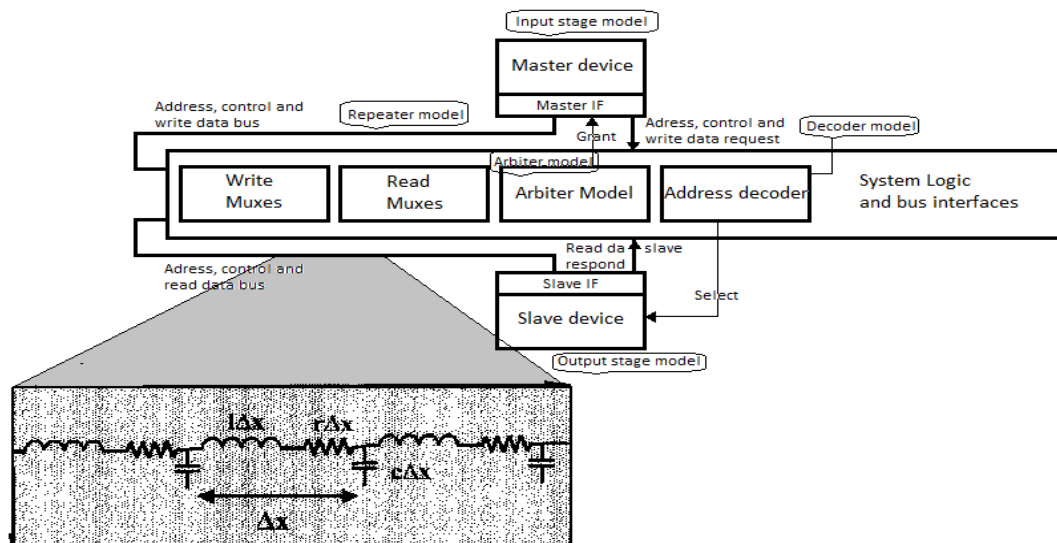


Figure 1.1: proposed model for power estimation

Power consumed in the system level are divided to:

- Power consumed in the Bus wire.
- Power consumed in the bus interface.

- Power consumed in the logic gate.

Power estimation in bus wire will be approached:

- High frequency with low system activity (minimum requirement to connect all system terminals).
- High frequency with high system activity.

In normal approach: develop an RLC model.

In high frequency approach: develop a high power level model.

## **1.6 Aim and Objectives:**

The main aim of this research to improve on chip communication Architecture Power Estimation in High Frequency high power model.

The main objective of this thesis is to study and understand the significance of on chip communication architecture, then design and modify the power estimation model in communication architecture and then simulate the proposed model in matlab to validate and verify the model accuracy.

## **1.7 Thesis Outline:**

Chapter two of this thesis gives a literature review for power estimation on SoC and gives an overview defining Network on Chip (NoC) and NoC architecture, chapter three introduces the used model and explain the system analysis and method used to estimate the power consumed on the SoC under study, chapter four presents the attained result of the analysis and measurement and discuss them briefly, chapter five concludes the thesis and signals recommendation that can be approached.