

**Sudan University of Science & Technology**  
**College of Graduated Studies**



**On chip communication Architecture Power  
Estimation in High Frequency**

تقدير الطاقة المستهلكة في نبيضة ذات معمارية اتصال مضمنة  
في نموذج تردد عالي

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degree of M.Sc in Communication Engineering

**By:**

*Khalid Bsheer Suliman*

**Supervised:**

*Dr Rashid A.Saeed*

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## الآية

”اقْرَأْ بِاسْمِ رَبِّكَ الَّذِي خَلَقَ ﴿١﴾ خَلَقَ الْإِنْسَانَ مِنْ عَلَقٍ ﴿٢﴾ اقْرَأْ وَرَبُّكَ الْأَكْرَمُ ﴿٣﴾ الَّذِي عَلَّمَ بِالْقَلَمِ ﴿٤﴾ عَلَّمَ

الْإِنْسَانَ مَا لَمْ يَعْلَمْ ﴿٥﴾“ صدق الله العظيم

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## Abstract

The development in embedded system on chip SoC is still evolving in its capabilities, to cover the everlasting needs in high edge technology over the world production and manufacturing, the development led to a plethora of SoC chip designs having high processing capabilities with high memory and interfaces all of this requirements increased the consumed power within the chip, bearing this in mind, we find all system designers over the world are optimizing power usage efficiency over the system chip due to its low power budget usage (E.g. batteries), based on all of this we find that a good power optimization system must be built over an accurate power estimation scheme.

This thesis proposes a power SoC estimation based on a system level analysis for a commercial piece of the art ARM Bus Architecture (AMBA chip), and that by decomposing the SoC chip power to the power consumed in (i) the logic element such as (arbiter, decoder, input devices and output devices) which called system devices which will be calculated by taking any device functionality in consideration such as (control signal and transitions), (ii) the chip bus and bus interface by developing a high frequency model using RLC component calculation for the bus wire, by bearing in mind system activity we use high level power model which presume that the bus power is consumed in the VIAS, the repeaters and the switching power, by implying these methods to the matlab we generated a power spectrum estimation in all system parts individually, by comparing the consumed power magnitude and amplitude in the system deferent parts we can understand the power consumption level which can help the designer in system evaluation and power optimization, it can be seen that using this method give us a hole on chip communication power estimation.

## المستخلص

لاتزال الانظمة المضمنة في الشريحة (SoC) تتطور في امكانياتها وذلك لكي تفي بالاحتياجات المتزايدة في مجالات تطوير وتصنيع التكنولوجيا الحديثة, هذه الاحتياجات جعلت المصممين يقدمون تصميمات كثيرة ذات امكانات هائلة في المعالجة وحجم الذاكرة و المقابلة, مع كل هذا التزايد في امكانات الشريحة زادت الطاقة المستخدمة في الشريحة مما يرفع من الحاجة لتحسين كفاءة استهلاك الطاقة داخل الشريحة وذلك مع معرفة ان اغلب هذه الانظمة المضمنة تعمل في بيئة عمل ذات طاقة منخفضة (مثلاً: الاجهزة الجواله - البطاريات) ونتيجة لكل هذا نجد انه من المهم كخطوة اولى تطوير طرق ذات كفاءة عالية لتقدير الطاقة المستهلكة داخل الانظمة المضمنة بالشرائح وذلك قبل القيام بأي عملية لتحسين استهلاك الطاقة بالشريحة.

تقدم هذه الاطروحة طريقة لتقدير الطاقة المستهلكة داخل شريحة SoC وذلك بالتحليل على مستوى النظام لواحدة من الشرائح التجارية الحديثة والمسماه المعمارية الخطية الحديثة للمتحمك الدقيق (AMBA), تم حصر الطاقة المستهلكة في الشريحة الى عدة اجزاء وهي: (1) العناصر المنطقية مثل (المحكم-المشفر- اجهزة الإدخال و اجهزة الإخراج) والتي تدعى اجهزة النظام ويتم حساب الطاقة بها بالأخذ في الاعتبار طريقة عمل هذه الاجهزة مثل عمليات الانتقال و التحكم, (2) اسلاك الخطوط و اجزاء المقابلة بالخطوط وذلك بتطوير نموذج للتردد العالي يحتوي على عناصر المقاومة المحاثة والمتسعة RLC لحساب الطاقة المستهلكة باسلاك الخط, عند النظر لنشاط النظام نقوم باستخدام نموذج مستوى الطاقة العالية والذي يقوم بحساب الطاقة المستهلكة في نقاط ارتباط الترانزستورات بين الطبقات (VIAS) و المكرر و طاقة التبديل, عند تطبيق هذه النماذج للماتلاب تم الحصول على تقدير لطاقة الطيف في كل اجزاء النظام, مما يساعد في فهم مستويات استهلاك الطاقة بالنظام.

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**Abbreviation:**

AHB	Advanced High Speed Bus
AMBA	Advanced Micro-controller Bus Architecture
CDFG	Control-Data-Flow Graphs
DPM	Dynamic Power Management
ECC	Error Correcting Codes
EMI	Electro-Magnetic Interference
ESL	Electronic System Level
GALS	Globally-Asynchronous Locally-Synchronous
HW/SW	Hardware and Software
ISS	Instruction Set Simulator
MPSoC	Multi-Processor Systems-on-Chips
NoC	Network on Chip
NP	Network Processors
P2M	Point to Multi
P2P	Point to Point
PCC	Parallel Computer Clusters
PDA	Personal Digital Assistance
PE	Processing Element
PMP	Parallel Media Processors
RTL	Register Transfer Level
SAN	System-Area Networks
SE	Storage Element
SIA	Semiconductor Industry Association
SoC	System on Chip
VLSI	Very Large Scale Integration