بسم الله الرحمن الرحيم

Sudan University of Science and Technology

College of Graduate Studies

Master of computer Engineering

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2D Radar antenna orientation and control

التوجية و التحكم الثنائي الأبعاد في هوائي الرادار

Prepared by:

Tayseer Mustafa Hummaida Abdalla

Supervised by:

Dr: Abdalrasool Gabar Alzubiadi.

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Approval Page

Name of Candidate: Tayseer Mustafa Hummaida Abdalla

Thesis title: 2D Radar antenna orientation and control

Approved by:

1. External Examiner

Name: Dr. Osman Ibrahim Osman Al-Aglan

Signature: ..... Date: 15/06/2015

2. Internal Examiner

Name: Dr. Mudathir Abdallah Osman Fagiri

Signature: Fagiri Date: 15/6/2015

3. Supervisor

Name: Dr. Abdelrasoul Jabar Alzubaidi

Signature: ..... Date: 15/6/2015

Sudan University of Science and Technology
College of Graduate Studies

Declaration

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التوجيه و التحكم الثنائي الأبعاد لهوائي الرادار

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Candidate's name: Taysеer Mustafa Hummaida AbdALLA

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إقرار

أنا الموقع أدناه أُقر بأننى المؤلف الوحيد لرسالة الماجستير المعنونة

التوجيه و التحكم ثنائي الأبعاد لهوائي الرادار

وهى منتج فكري أصيل . وباختياري أعطى حقوق طبع ونشر هذا العمل لكلية الدراسات العليا - جامعه السودان للعلوم والتكنولوجيا، عليه يحق للجامعه نشر هذا العمل للأغراض العلمية .

اسم الدارس : تيسير مصطفى حميدة عبدالله

توقيع الدارس : ..... التاريخ: 25/8/2015

الآية

بسم الله الرحمن الرحيم

﴿إِنْ أُرِيدُ إِلا الإِصْلاحَ مَا اسْتَطَعْتُ وَمَا تَوْفِيقِي إِلا بِاللهِ عَلَيْهِ تَوَكَّلْتُ وَإِلَيْهِ أُنِيبُ﴾

(هود/88)

الإهـــداء

إلى من اوصاني ربي بهما خيرا إلى من كانت دعواتهما لي بالسر والعلن
إلى قدوتي ومن شجعني على مواصلة مسيرتي العلمية
خير الزاد أبي الغالي وأمي الحنونة اطال الله في عمرهما
إلى رياحين حياتي في الشدة والرخاء
أخوتي.....
وأخواتي.....
وإلى كل من شجعني وساعدني على إتمام هذا العمل.

ABSTRACT

In the RADAR system is first step and much more important and it much more effect in the other step in RADAR system works.

The RADAR is used in different applications and systems, almost of these applications need high precision, and it's depending on accuracy of RADAR ANTENNA orientation. Many researches have been done and different systems designed to obtain the result within permissible range. Design RADAR ANTENNA orientation and control system using FPGA and stepper motor. The control system is modeled to monitor and control the antenna in the azimuth (Horizontal axis) and elevation.

Different initial position of RADAR antenna ‹to evaluate system performance. based on different scenarios of initial position which were implemented by the main circuit of the RADAR ANTENNA orientation and control system.and the antenna is orientation to the north (0◦).

شكر وعرفان

قال تعالى { وَقَالَ رَبِّ أَوْزِعْنِي أَنْ أَشْكُرَ نِعْمَتَكَ الَّتِي أَنْعَمْتَ عَلَيَّ وَعَلَى وَالِدَيَّ وَأَنْ أَعْمَلَ صَالِحاً تَرْضَاهُ وَأَدْخِلْنِي بِرَحْمَتِكَ فِي عِبَادِكَ الصَّالِحِينَ }النمل19.

الشكر والمنة والحمد لله أولاً على ما هدى ووفق وسدد. فإني مدين بالشكر لكل من قدم إلي يد العون خلال مسيرة تعليمي من أساتذة وأقارب وأصدقاء، وارشدني في كتابة هذا البحث المتواضع فلهم مني الشكر والتقديربعد شكر الله عز وجل.

الشكر والتقدير لأساتذي الجليل المشرف الأول أ.د/ عبد الرسول الزبيدي الذي اشرف على هذا البحث منذ أن كان فكرة وكذلك يطيب لي أن أشكر كل من وضع بصمات بيضاء في هذا البحث و يتصل الشكر لأساتذتي و كل من علمني حرفاً..

الباحث

المستخلص

في انظمة الرادار يشكل توجية هوائي الرادار المرحلة الاولي و الأهم و التي تؤثر بشكل كبير في صحة و دقة بقية مراحل عملها . و لأن الرادار يستخدم في كثير من المجالات و التطبيقات،و معظم التطبيقات تحتاج دقة عالية ، وهذا يعتمد على التوجية الدقيق لهوائي الرادار لذا اجريت كثير من الابحاث و صممت انظمة مختلفة للحصول على نتائج في حدود الدقة المسموح بها .

و لتحقيق تلك المتطلبات، صمم نظام التوجية و التحكم في هوائي الرادار على محورين (الأفقي،الرأسي) .حيث صمم النظام بإستخدام مصفوفة البوابات القابلة للبرمجة (FPGA) كمتحكم رئيسي في النظام بالتحكم في حركة محرك الخطوة(stepper motor).

اخدت قيم مختلفة للإحداثيات الابتدائية لهوائي الرادار تم تقيم اداء النظام عن طريقها .و بناء علي السناريوهات المختلفة للإحداثيات الابتدائية و التي تم تطبيقها عن طريق الدائرة الرئيسية لنظام التوجية و التحكم في هوائي الرادار. وجد ان الهوائي تم توجهة للشمال الجغرافي(0°) .

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List of abbreviation

DSP :Speed Digital Signal Processor.

ASIC :Application-Specific Integrated Circuit.

I/O :Input output.

MCU: Micro Controller Units.

2D: Two diminutions.

RADAR: Radio Detection and Ranging.

FPGA: Field Programmable gate array.

TXR: Transmitter and Receivers.

PWM: Pulse Width Modulation.

GUI: Graphic User Interface.

PPI: plan Position Indicator.

ADC: Analog to Digital convertor.

CLB:Configurable Logic Block

RAM: Random Access Memory.

LED: Light Meting Diode.

TTL:Transistor–transistor logic.

CMOS:Complementary metal–oxide–semiconductor.

DC: Direct current.

GND:Ground.

WAN:wide area network.

LAN:local area network.

CHAPTER

ONE

1.1Background:

Control systems are integrated into many facets of life; begin from nature to social issues to mechanical systems. A nature example would be our bodies: when we want to grab an object, our eyes will focus on it and relay the information to our brain, which will send electrical signals to our muscles to position our arms correctly. There are an unlimited number of control examples in the world, but we will focus on a particular control system (radar antenna control system).

The main goal of an antenna is to gather and convert electromagnetic waves to electronic signals. The coming designed antennas, radio telescopes, and telescopes have to satisfy control and pointing requirements that challenge existing technology.

In order to increase the data rate, the antennas are required to communicate at higher radio frequencies: from S-band (2.3 GHz) to X-band (8.5 GHz) to Ka-band (32 GHz). The increased frequency requires more precise antenna pointing systems and the increased size creates multiple pointing and control challenges.

The main objective of this research is modeling the orientation and control system for azimuth and elevation axis for antenna. Antennas are positioned at different geographical location and different terrains; the wind plays a major roll-on the system which creates major problems for antenna pointing mechanism. Hence determine the tilt in X and Y axis.

Controlling the motors with high-performance motor drives significantly improves the efficiency of these motors, thus lowering energy consumption. Better control also means one can select a smaller, more efficient motor for the same task– reducing the cost of the equipment.

Today's drives are typically multi-chip solutions; a high speed Digital Signal Processor (DSP) for fast math-intensive computation, an Application-Specific Integrated Circuit (ASIC) for industrial networking, and a processor to run the slower control loops and do all the other interfacing and I/O. But these drives typically run in a slow processor with fixed point control loops. They mainly support a single axis. Flexibility of design is primarily from software optimization.

The trend for next generation drives calls for a more integrated solution – that brings together the performance of an embedded dual-processor system, DSP blocks capable of floating point computation, and the scalability to add multiple motors in the same drive, thus lowering the cost per motor.

FPGAs are the ideal solution for these next generation drives– as programmability provides the ability to integrate more functions for additional flexibility and scalability. FPGAs also execute multiple operations in parallel, unlike MCU and DSP which are sequential machines, i.e. they execute one instruction at a time. The parallel nature of FPGA operation allows for higher speed computations therefore improving control performance.

FPGAs are a good fit for high end motor control because of the high performance motor control algorithms that can be implemented in a FPGA due to the inherent parallelism of the FPGA operation. In contrast, Micro Controller Units

(MCUs) and DSPs, being sequential machines, have a tough time keeping up when very high-speed runtime updates are needed in certain motor control algorithms, or when a number of motors need to be simultaneously controlled (multi-axis).

1.3 Problem Statement:

The newly designed antennas have to satisfy control and pointing requirements that challenge existing technology. And antennas are positioned at different geographical location and different terrains; the wind plays a major roll-on the system which creates major problems for antenna pointing mechanism.

1.4 Objective:

The main objective is to design a 2D radar antenna control and orientation system to utilize the maximum precise orientation. To achieve this objective:-

1. A control circuit for 2D radar antenna control and orientation using transmitter point (*Tx*R) and FPGA will be proposed.
2. Control system for azimuth and elevation axis for antenna using stepper motor.
3. Control algorithm will be used so as to minimize the error.
4. Simulation of the proposed system will be run.
5. Implementation of a pro-type system will be done.
6. Performance evaluation for the system will be done.

1.5 Methodology:

A FPGA based radar antenna control and orientation system is proposed to:

1.5.1 Orientation the antenna:

It's the main and first step in the proposed system:

In the beginning, a signal is send to the antenna by the transmit point, which is built in fixed point and it have the same frequency of antenna. Then the signal is read in PPI and it'll be checked whether it's in the zero's degree and it'll be set by controlling the driver to get precise orientation of antenna.

1.5.2 Controlling drive speed:

The drive speed is ultimately controlled by the torque changes induced by varying FPGA logic applied to the motors. In order to control elevation and azimuth based in the application of the system.

1.6 Research Outline:

I. Literature review on the orientation and control of radar antenna and control of stepper motor.
II. Electronic circuit design of (FPGA based 2D radar antenna orientation and control) using stepper motor.
III. Software programming of the (FPGA based 2D radar antenna orientation and control)circuit using VHDL language
IV. Result and discussion of the implementation of (FPGA based 2D radar antenna orientation and control) system.
V. Conclusion and recommendation.

CHAPTER

TOW

2.1 Literature review:

Several works have been done in the area of radar antenna orientation and control system and stepper motor control, among them; these are the most recent researches:

Study undertaken during 2014 at the RV College of Engineering, Bangalore, India. The study conclude that there is In order to speed up the data rate, the antennas are required to operate at higher radio frequencies. The increased frequency requires more precise antenna pointing system and the need of pointing control is to counter act the effect of external disturbances which includes wind gust, terrain profile etc. All these factors demand an embedded system engineer to design a more accurate antenna control system. This paper describes the control system engineering principles used in designing, testing and implementing, a control and measurement system on an antenna. The control system is modeled to monitor and control the antenna in elevation (Vertical axis) and azimuth (Horizontal axis). The system is also stabilized with the help of level sensor [1].

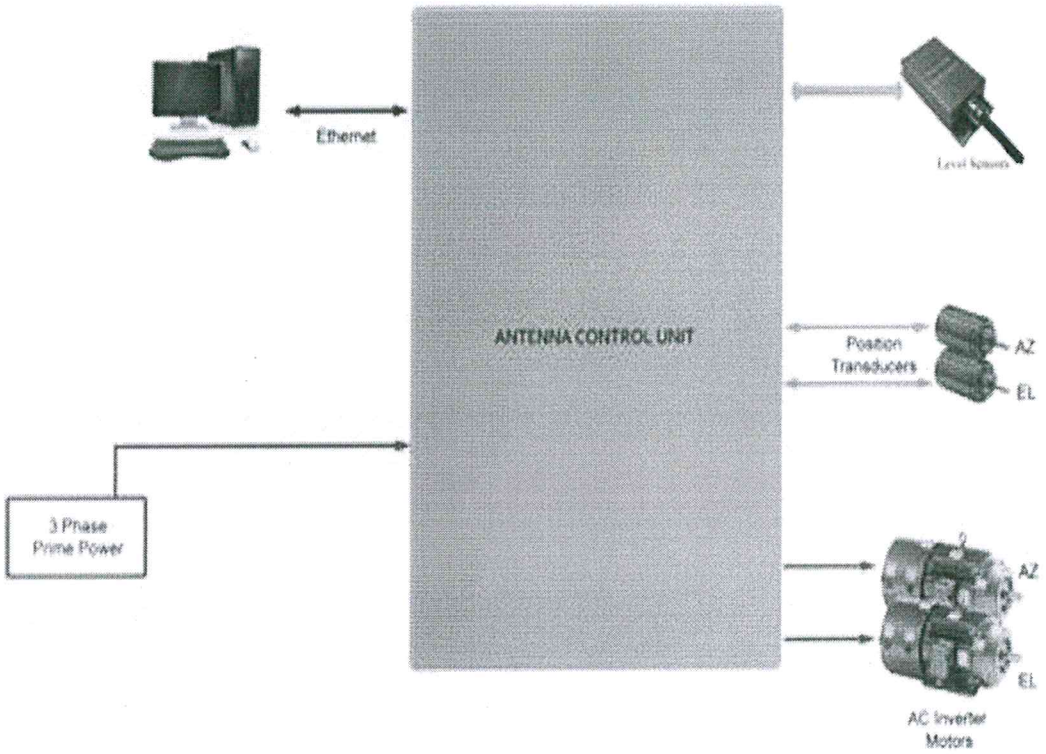

Figure2. 1 control and measurement system on an antenna system

Other Study during 2014 at the Military Academy. The study about the antenna azimuth position control system turns the input command in output position. This system is widely used in antennas, robots and computers disks. In this paper we present the systems that are managed with azimuth antenna. We're going to show how the system works and how its performance can be improved. The purpose of this system is the input angle to be turned into an output angle of the antenna [2].

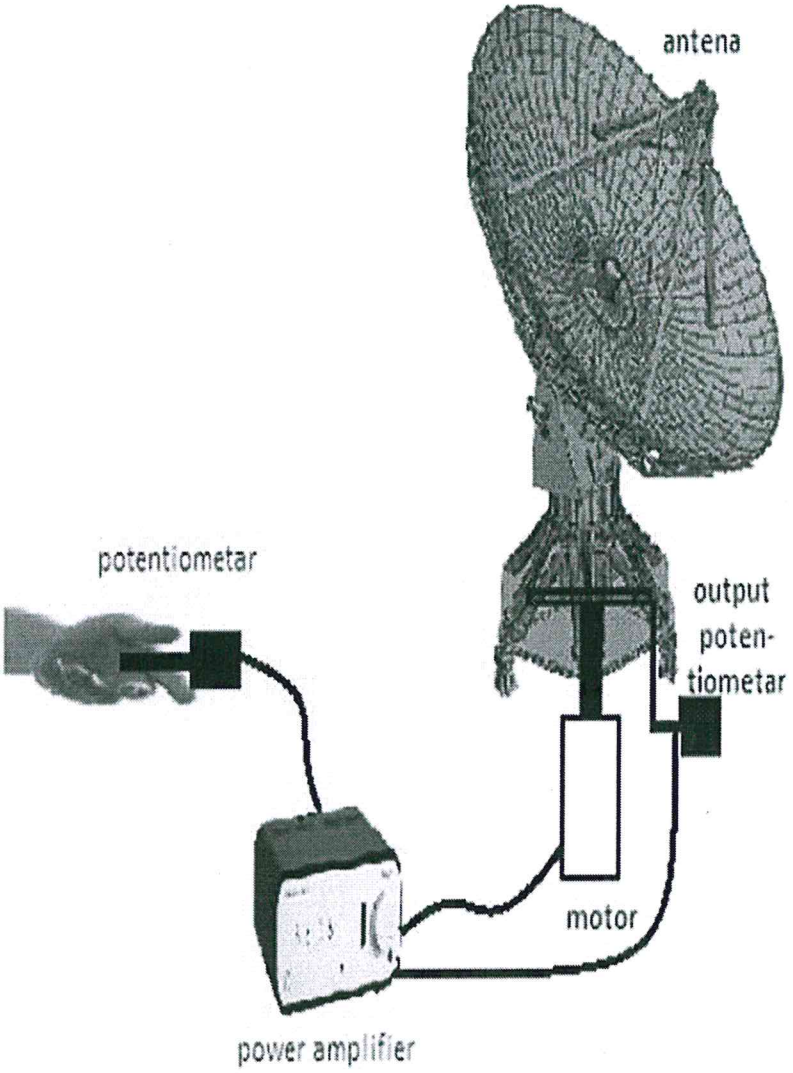

Figure2. 2 antenna azimuth position control system

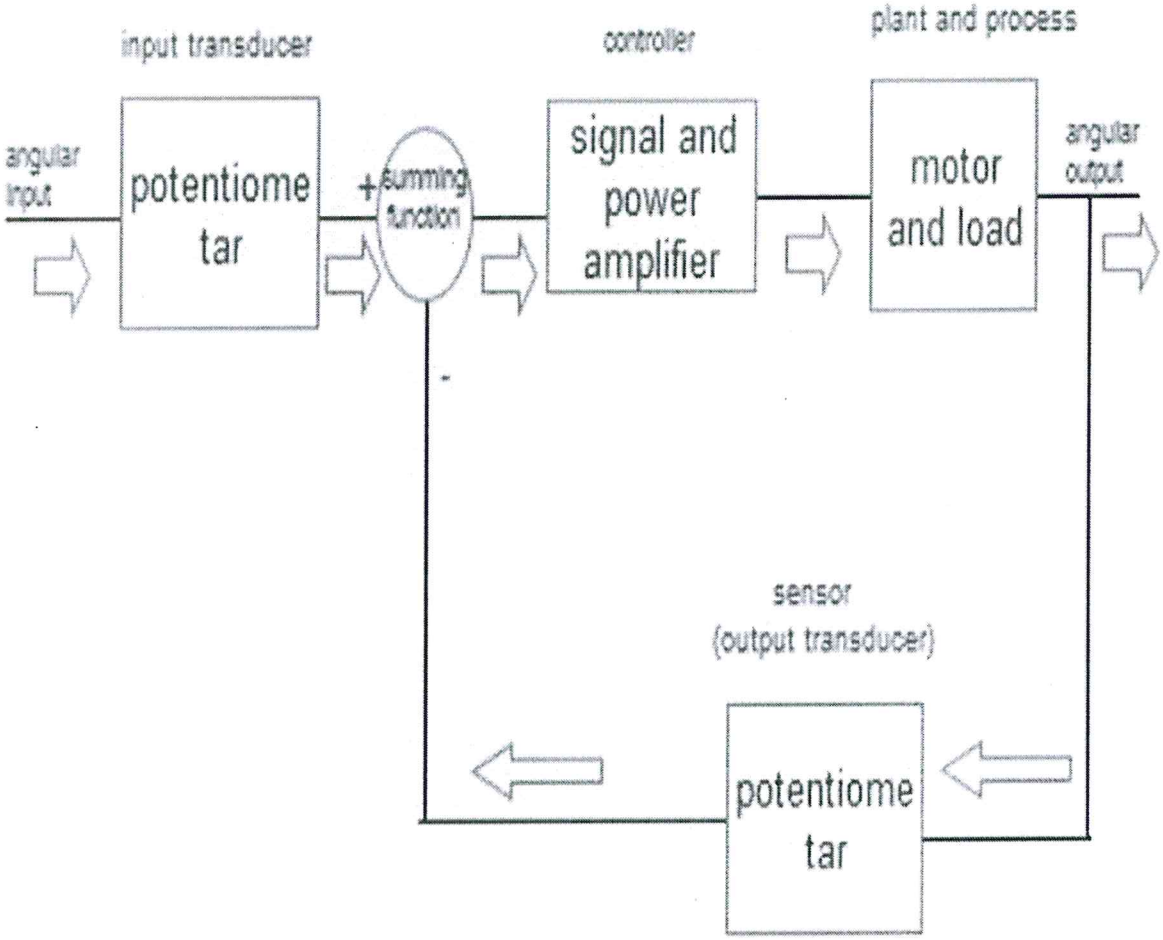

Figure2. 3 antenna azimuth position control system block diagrams

Third Study during 2005 for improving the control system of some bio-chemistry analysis instrument, an approach of micro-stepping control for the step motors based on field programmable gate array (FPGA) is presented after the micro-stepping driving theory of the step motor with a constant torque was discussed deeply. And then the relative control system is schematically designed, mainly includes the internal logic design of the FPGA, the communication interface design of the microcomputer, the design of the power driving circuit, and the design of the interface circuit between the electrical sources. At last, it is verified by some experimental investigations that the control theory and approach presented in the paper are corrective, and the control system designed is very good to get a high precision of position

control and high control repeatability. So the technology questions from the producing reality are resolved and the product quality is promoted [3].

Also Study during 2007presented an open loop stepper motor driver using a FPGA. The model of the current controller is described and gains of the PI controller are selected at optimal values. In this design, the FPGA is used to build a high performance open loop driver without using a DSP; furthermore it is compatible with ASICs and mass production methods. The experimental results verify the performance of the driver [4].

In addition Study during 2005 presented. Wireless stepper motor controller designed using Very High Speed Integrated Circuit Hardware

Description Language (VHDL) and is implemented on SPARATAN Field Programmable Gate Array (FPGA). The Proposed motor controller is controlled by using Pulse Width Modulation Technique (PWM) thus giving the very high precision. Due to high torque of stepper motor it is capable of handling the big industrial automation system. In this system GUI will be designed using LABVIEW to give the control parameter to the wireless connected stepper motor.

Same system can also be used in the mobile robot, functioning in the hazardous area and can be very well equipped with the nuclear reactor to control the movement of control rod. One of the best use is to track solar energy because the resolution of stepper motor will be highly increased i.e. 0.915°.

This paper describes a stepper motor controller designed using VHDL and implemented in FPGA. The system is capable of controlling the stepper motor in terms of step angle at 0.915°. In addition to this we can make it to rotate at different – different speeds, displacement clockwise and anticlockwise direction wirelessly. Here GUI is designed for inputting the

user defined control parameter to faithfully control the system in industrial automation.

One of the major advantages of using LABVIEW is, it acts as a virtual instrument, thus reduces the cost of project by eliminating the necessity of making control panel. It is user-friendly reduces programming complexity and errors can be easily identified and rectified [5].

CHAPTER THREE

3.1 Overview:

In this chapter the researcher is going to design final electronics circuit design of control system. The electronic circuit composes of many components; the basic unit is FPGA kit, uln2003, stepper motor, microstepper motor, TXR point and researcher will talk briefly about each previous mentioned component.

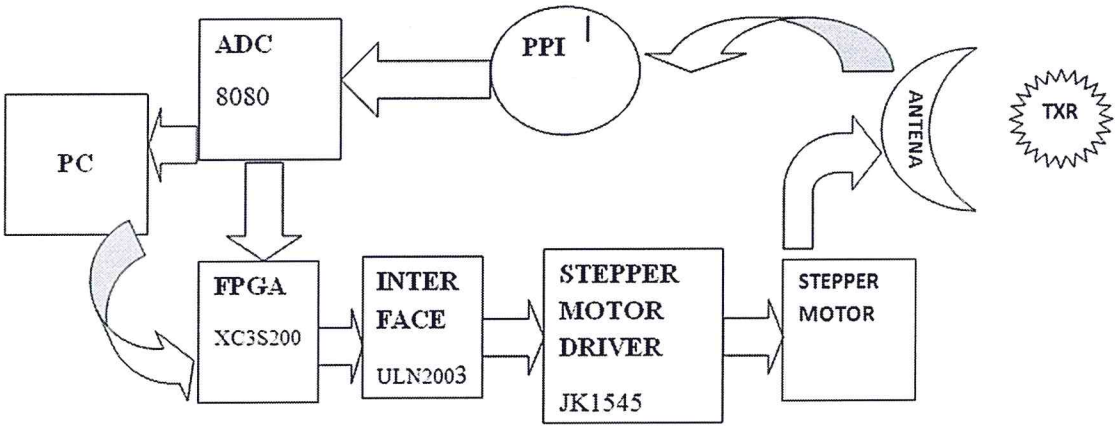

Figure3. 1 electronics circuit block diagrams

3.2 FPGA Kit:

The researcher used the Xilinx Spartan -3E FPGA kit to design simple 2D radar antenna orientation and control which can be further developed to perform more precise radar antenna orientation and easy control. The core component of FPGA is 200k gate Xilinx Spartan – XC3S200E, the chip has many specific features and component. FPGA consists of many parts:

3.2.1 Key components & features:

XC3S_200, which includes the following components and features as figure (4.1) show:

- 2000K System Gate.
- 4,320 Equivalent Logic Cells.
- CLB Array (One CLB = Four Slices), 24 Rows, 20 Columns, 480 Total CLBs.
- 30K Distributed RAM Bits (K=1024).
- 216K Block RAM Bits (K=1024).
- 12 Dedicated Multipliers.
- 4 DCMs.
- 173 Max User I/O.
- 76 Maximum Differential I/O Pairs.

3.3 ULN2003 High Voltage and High Current

Darlington transistor array:

3.3.1 Description:

The ULN2003 is a monolithic high voltage and high current Darlington transistor arrays. It consists of seven NPN darlington pairs that features high-voltage outputs with common-cathode clamp diode for switching inductive loads. The collector current rating of a single darlington pair is 500mA. The darlington pairs may be parrlleled for higher current capability. Applications include relay drivers,hammer drivers, lampdrivers,display drivers(LED gas discharge),line drivers, and logic buffers.

The ULN2003 has a 2.7kW series base resistor for each darlington pair for operation directly with TTL or 5V CMOS devices.

3.3.2Feature:

* 500mA rated collector current (Single output).

* High-voltage outputs: 50V.

* Inputs compatible with various types of logic.

* Relay driver application.

3.3.3 Logic diagram:

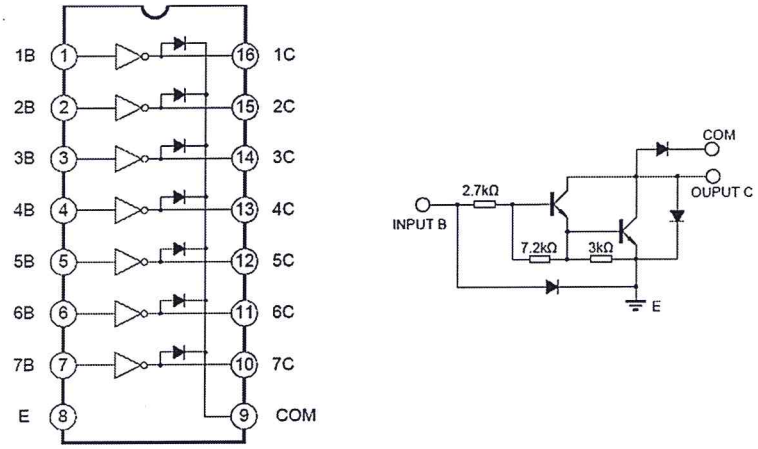

Figure3. 2 ULN2003 block diagrams

3.4 JK1545 2-Phase Stepper Motor Driver:

3.4.1 Characteristics :

1. DC power input type: 24V-50VDC.

2. Output current: 1.3A-4.5A.

3.Mircostepping : 1(1.8°),1/2,1/,1/8,1/16,1/32,1/64,1/128,1/256

1/5, 1/10, 1/25, 1/50, 1/125, 1/250.

4. Protect form: Overheated protect, lock automatic half current, error connect protect

5. Dimensions : 118mm×76mm×33mm

6. Weight : <300g.

7. Working environment: Temperature 15-40℃ Humidity<90%.

3.4.2 I/O Ports :

1. VCC+ : DC power positive pole.

Note: Must guard against exceeding 50V, so as not to damage the module

2. GND : DC power cathode.

3. A+、A- : Stepping motor one winding.

4. B+、B- : Stepping motor other winding.

5. PUL+, PUL - : Stepping pulse input+5V (Rising edge effective, rising edge duration >10μS).

6. DIR +、DIR- : Stepping motor direction input, voltage level touched off, high towards, low reverse.

7. ENA+、ENA-: motor free.

3.4.3 Microstepping choice:

Switch Choice: (ON=0, OFF=1)

SW5	0	0	0	0	0	0	0	0	1	1	1	1	1	1
SW6	0	1	0	1	0	1	0	1	0	1	0	1	0	1
SW7	0	0	1	1	0	0	1	1	0	0	1	1	0	0
SW8	0	0	0	0	1	1	1	1	0	0	0	0	1	1
Micro	1/2	1/4	1/8	1/16	1/32	1/64	1/128	1/256	1/5	1/10	1/25	1/50	1/125	1/250

Table (3.1) JK1545 Microstepping choice

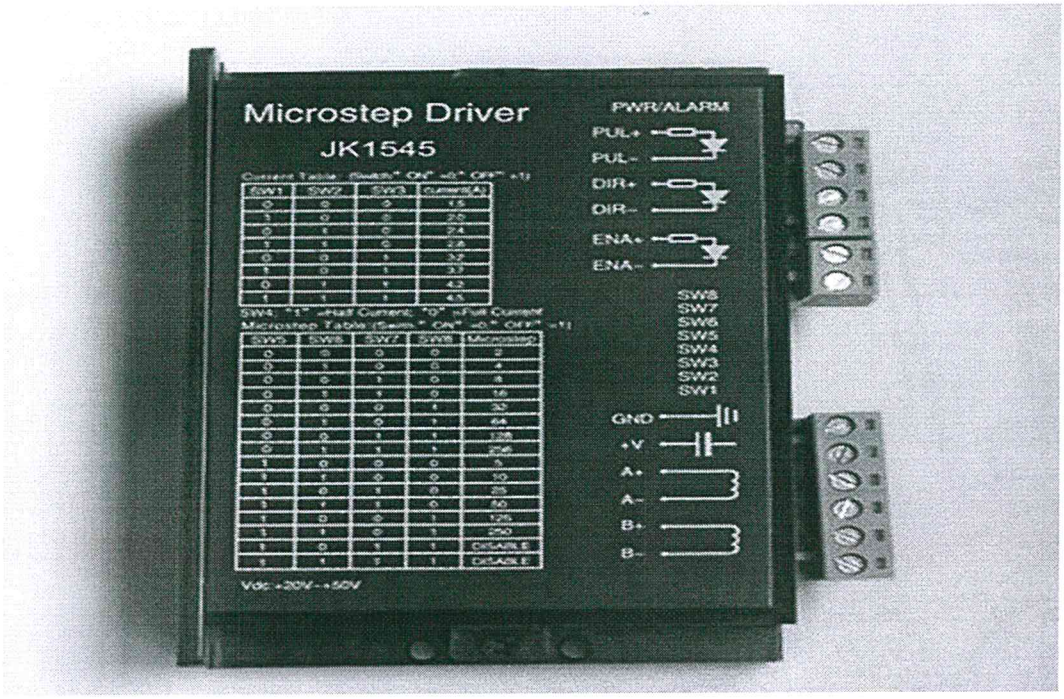

Figure3. 3 JK1545 2-Phase Stepper Motor Driver

3.5 Stepper motor:

A stepper motor is used for the procedure of orientation of the antenna of the Radar .The number of steps of the stepper motor is (200 steps / revolution). Equation (1) gives the value of the step angle of the stepper motor.

Step angle = One revolution /200

= 3600 Step/200 = 1.8 Degree

3.6 Analog-to-digital converter (ADC0808/ADC0809):

3.6 .1General description:

The ADC0808, ADC0809 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 8-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 8-channel multiplexer can directly access any of 8-single-ended analog signals.

The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE® outputs.

The design of the ADC0808, ADC0809 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0808, ADC0809 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications from process and machine control to consumer and automotive applications. For 16-channel multiplexer with common output (sample/hold port) see ADC0816 data sheet.

3.6.2 Features:

- Easy interface to all microprocessors
- Operates ratio metrically or with 5 VDC or analog span
- adjusted voltage reference
- No zero or full-scale adjust required
- 8-channel multiplexer with address logic

- 0V to 5V input range with single 5V power supply
- Outputs meet TTL voltage level specifications
- Standard hermetic or molded 28-pin DIP package
- 28-pin molded chip carrier package
- ADC0808 equivalent to MM74C949
- ADC0809 equivalent to MM74C949-1

3.6.3 Key specifications:

- Resolution 8 Bits
- Total Unadjusted Error ±1/2 LSB and ±1 LSB
- Single Supply 5 VDC
- Low Power 15 mW
- Conversion Time 100 μs

3.6.3 Block diagram:

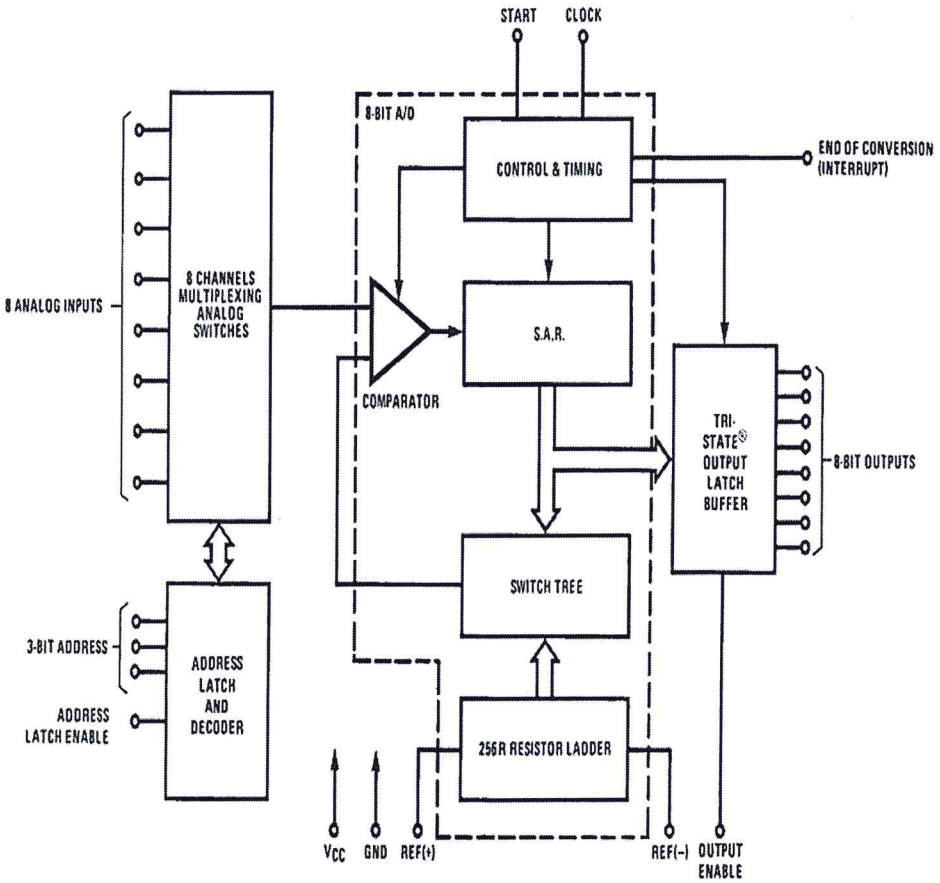

Figure3. 4 ADC0808/ADC0809 block diagram

3.6.4 Connection diagrams:

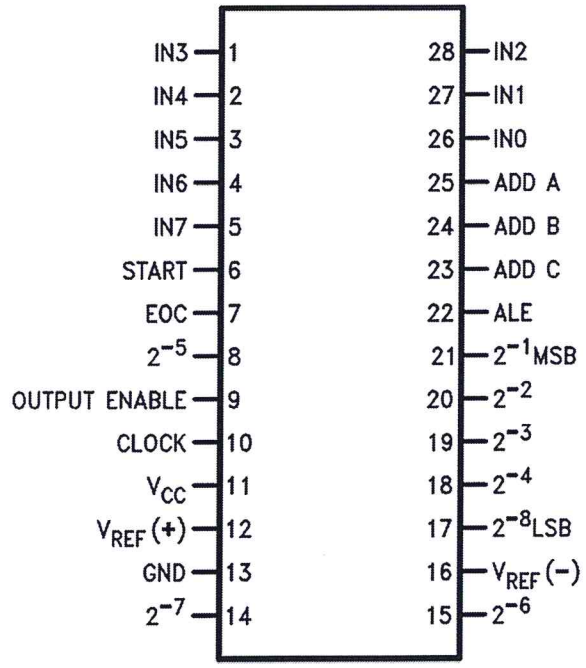

Figure3. 5 ADC0808/ADC0809 block diagram

3.7 The antenna:

A parabolic antenna is an antenna that uses a parabolic reflector, a curved surface with the cross-sectional shape of a parabola, to direct the radio waves. The most common form is shaped like a dish and is popularly called a dish antenna or parabolic dish.

Parabolic antennas are used as high-gain antennas for point-to-point communications, in applications such as microwave relay links that carry telephone and television signals between nearby cities, wireless WAN/LAN links for data communications, satellite communications and spacecraft communication antennas. They are also used in radio telescopes.

The other large use of parabolic antennas is for radar antennas, in which there is a need to transmit a narrow beam of radio waves to locate

objects likes ships, airplanes, and guided missiles. With the advent of home satellite television receivers, parabolic antennas have become a common feature of the landscapes of modern countries.

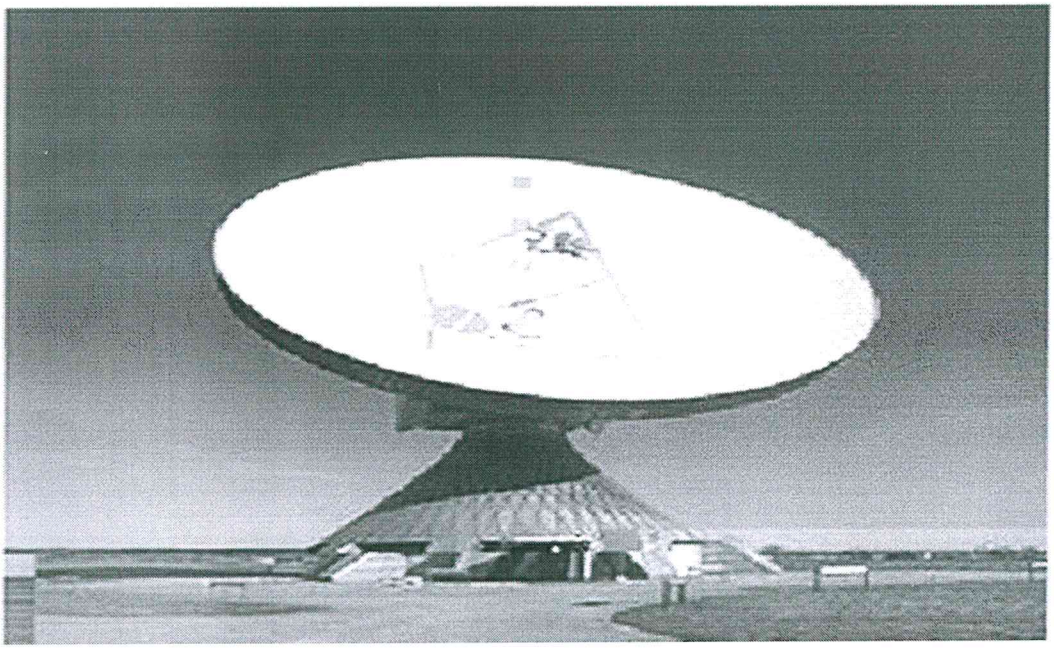

Figure3. 6 parabolic antenna

3.8 Plan position indicator (PPI):

The plan position indicator (PPI), is the most common type of radar display. The radar antenna is usually represented in the center of the display, so the distance from it and height above ground can be drawn as concentric circles. As the radar antenna rotates, a radial trace on the PPI sweeps in unison with it about the center point.

The PPI-scope shown in figure3.7 is by far the most used radar display. It is a polar coordinate display of the area surrounding the radar platform. Own position is represented as the origin of the sweep, which is normally located in the center of the scope, but may be offset from the center on some sets. The ppi uses a radial sweep pivoting about the center of the presentation.

The sweep rotates on the display just as fast as the radar antenna. This results in a map-like picture of the area covered by the radar beam. A long-persistence screen is used so that the targets remain visible until the sweep passes again.

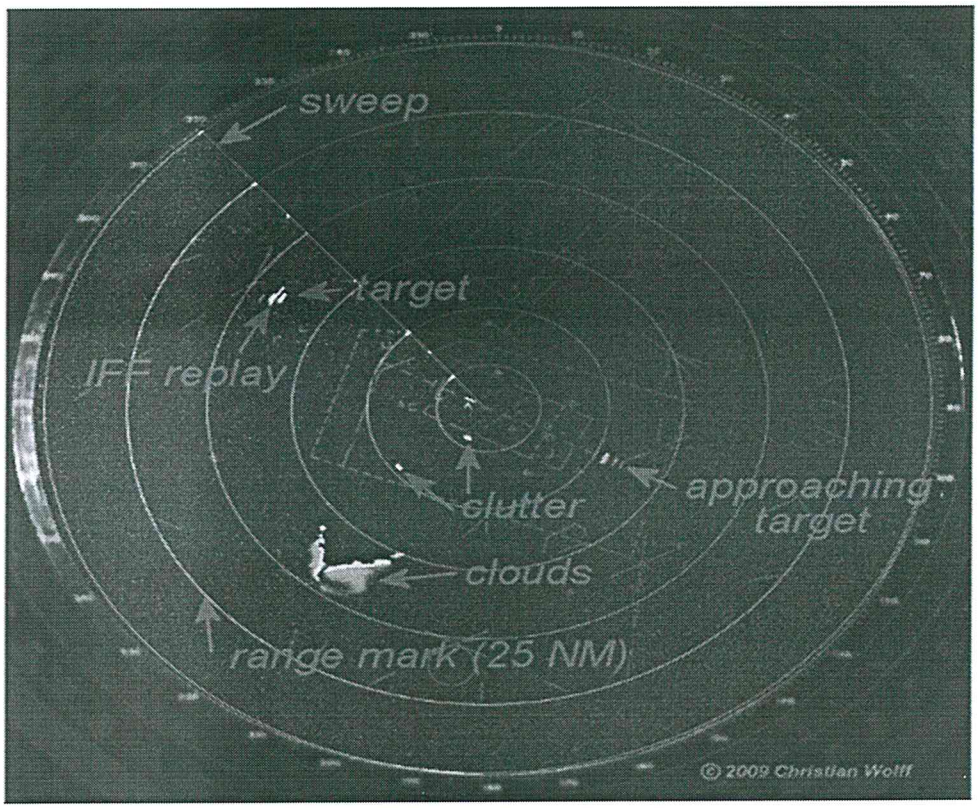

Figure3. 7 plan position indicator (PPI)

3.9 Wireless Transmitter and Receiver:

It used as a source of signal when started the process of orientation to the antenna, and be fixed at the geographical North

CHAPTER FOUR

4.1 Overview:

In this chapter, the researcher going to give brief explanation of the software program that used to operate it in my control circuit. Whenever there software to guide, the hardware should be used to complete the interface and control process.

A Very High Speed Integrated Circuit Hardware Description Language (VHDL) is implemented on SPARATAN Field Programmable Gate Array (FPGA).

VHDL language allows the system to be described at many different levels, from the lowest level of the logic gate through the behavioral level. VHDL is intended for circuit's synthesis as well as circuit simulation. However, VHDL is fully simulated, and not all constructions are synthesizable.

A fundamental motivation to use VHDL that VHDL is a standard, technology independent language, therefore, portable and reusable. The two main immediate applications of VHDL are in the field programmable logic devices (including CPLD – complex logic devices) and field programmable gate arrays (FPGA) and in the field of ASIC (application specific integrated circuits). Once the VHDL code has been written, it can be used either to implement the circuit in the programmable device or can be submitted to foundry for fabrication of an ASIC chip.

4.2 Software Program & Algorithms:

The algorithm is based on supplying the FPGA through the ADC with the azimuth angle appeared on the PPI of the Radar in the digital format .The FPGA in its turn processes the data and issues a correction command to the stepper motor in order to align the antenna to the geographical north (0◦) .

4.2.1Orientation procedure:

The orientation procedure of the Radar antenna is as follows:

- The transmitter issues a signal.
- The PPI of the Radar displays the transmitter signal as a dummy target on the PPI.
- The ADC transforms the DC voltage into digital format.
- The FPGA processes the digital data.
- The FPGA issues correction command to the stepper motor through the interface.
- The stepper motor aligns the antenna to the geographical north (0◦).

VHDL programming language is used for programming the FPGA by the computer the algorithm is:

Start

Initialization:

- Program port (A1) of FPGA as input.
- Program port (A2) of FPGA as output.
- Put transmitter mode to (OFF).
- Adjust the plane position indicator (PPI) of the Radar to the geographical north (0◦).
- Clear output to stepper motor.

Processing:

- Put transmitter mode to (ON).

- Call orientation subroutine.
- End

Orientation subroutine:

Blip detection:

- Observe the blip on the PPI of the Radar.
- Check the incoming azimuth and elevation value of the blip.
- If the azimuth value equals zero, then go to terminate the subroutine.
- If the azimuth value does not equal zero, then go to antenna position correction.
- Go to blip detection.

Antenna position correction:

- If the azimuth value is positive, then rotate the stepper motor one-step anticlockwise.
- If the azimuth value is negative, then rotate the stepper motor one-step clockwise.
- Go to blip detection.

Terminate:

Return.

CHAPTER FIVE

5.2 RESULTS AND DESCUSSION:

A transmitter tuned to the Radar receiver frequency is used to generate a blip (dummy target) on the PPI display of the Radar. when applying the algorithm in paragraph chapter four above, we observe the location of the blip on the PPI .Based on the blip azimuth and elevation angle, the program in the FPGA performs the alignment of the antenna with the blip appearance on the PPI of the Radar .The alignment processing continues till we get the antenna exactly heading to the geographical north (0 Degrees). Each step movement of the stepper motor makes an antenna azimuth angle correction of (1.8 Degrees) .A microstep driver is implemented to enhance the stepper motor angle resolution up to of (0.007Degrees).

CHAPTER

SIX

6.1 Conclusion:

The functionality of the design starts with activating a transmitter tuned to the Radar frequency. A dummy blip (target) appears on the PPI display of the Radar. Any antenna azimuth angle deviation from the geographical north will be subjected to correction procedure. Based on the blip appearance on the PPI, the FPGA program performs the correction by commanding the stepper motor to rotate clockwise or anticlockwise. The processing outcome is to put both the antenna and the PPI display on (0_0). The alignment procedure (orientation) makes us avoiding azimuth and elevation data capture errors by the Radar.

6.2 Recommendations:

Here are many issues related to RADAR ANTENNA orientation and control that could be subject to further studies:

-it will be better to use sun tracking to antenna orientation .

-in this research, orientation and controlling radar antenna was discussed via controlling stepper motor by FPGA and the researcher recommends that to use components with more speed and precise.

Reference:

[1]. Mr.N.Sai Pavan, Mr.Ramavenkateswaran.N: MODELLING OF THE STABILIZATIONAND TRACKING CONTROL SYSTEM FOR ANTENNA, *International Journal of Advanced Research in Computer and Communication Engineering , June 2014.*

[2]. Boban Temelkovskia and Jugoslav Achkoskia "Modeling and Simulation of Antenna Azimuth Position Control System "International Journal of Multidisciplinary and Current Research,2014.

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[4]. Ngoc Quy Le1 and Jae Wook Jeon2" An Open-loop Stepper Motor Driver Based on FPGA" International Conference on Control, Automation and Systems 2007Oct. 17-20, 2007 in COEX, Seoul, Korea

[5]. Arvind Kumar1, Mrs. M. Valarmathi2" High Precision Stepper Motor Controller Implementation on FPGA with GUI on LabVIEW"International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering *Vol. 2, Issue 4, April 2013.*

[6]. Tayseer Mustafa Hummaida 1, Abdelrasoul Jabar Alzubaidi 2, Yousif Taha Yousif Elamin 3."Orientation of Radar Antenna" *IOSR Journal of Electrical and Electronics Engineering (IOSR-JEEE). Jan – Feb. 2015.*

Appendixes A:

FPGA Configuration:

VHDL code:

```
-- Company:sust
-- Engineer: tayseer
--
-- Create Date:    14:59:41 05/11/2015
-- Design Name:
-- Module Name:    tayseer - Behavioral
-- Project Name:
-- Target Devices:
-- Tool versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
```

```
----------------------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
---- Uncomment the following library declaration if instantiating
---- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;
entity tayseer is
   Port ( a : in  STD_LOGIC_VECTOR (03 downto 0);
          b : out  STD_LOGIC_VECTOR (03 downto 0);
          clk : in  STD_LOGIC;
          led : out  STD_LOGIC_VECTOR (03 downto 0));
end tayseer;
architecture Behavioral of tayseer is
begin
process(clk) begin
  case a is
 when "0001" => b <=  "0001" ; led <= "0001";
 when "0010" => b <=  "0010";
 when "0100" => b <=  "0100";
 when "1000" => b <= "1000";
```

```
  when others => led <= "1111";

  end case;

end process;

end Behavioral;
```

Orientating and Control Code:

```
#include<stdio.h>
#include<conio.h>
#include<dos.h>

/* This program is written by Eng. Tayseer */
main()
{
/* initialisation */
int x;
/* put all output devices off */
outportb(0x378,0x00);

/* title for the thesis */
textmode(1);
gotoxy(5,2);
textcolor(WHITE);
textbackground(RED);
cprintf("\n TAYSEER   ");

gotoxy(5,6);
cprintf("\n    SUDAN  UNIVERSITY ");

gotoxy(5,10);
cprintf("\n orientation              ");

gotoxy(5,14);
cprintf("\n       start operation     ");

struct date d;
getdate(&d);
```

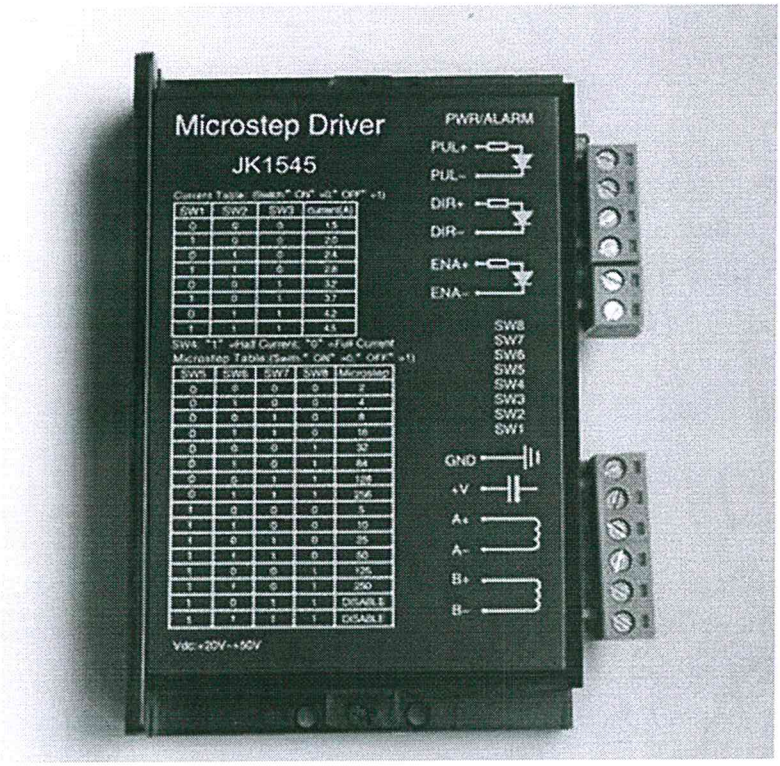
```
printf("\n\n %d / %d / %d", d.da_day, d.da_mon,d.da_year);
delay(5000);

screen2:
int xclockwise = 0;
clrscr();
textcolor(WHITE);
textbackground(BLUE);
gotoxy(5,2);
cprintf("\n   start counting the no. of steps ");


xclockwise:
if (kbhit()) goto stopstepper;

outportb(0x378,0x08);
delay(2000);
xclockwise=xclockwise+1;

outportb(0x378,0x04);
delay(2000);
xclockwise=xclockwise+1;

outportb(0x378,0x02);
delay(2000);
xclockwise=xclockwise+1;

outportb(0x378,0x01);
delay(2000);
xclockwise=xclockwise+1;
goto xclockwise;


stopstepper:
outportb(0x378,0x10);/* activate a siren*/
delay(3000);
outportb(0x378,0x00);/* dis-activate a siren*/
/* display the direction (the step considered is 1.8 degrees)*/

cprintf("\n The number of steps is:%d ", (xclockwise ));
```

```
gotoxy(7,12);

delay(10000);

screen3:
/*clrscr(); */
textcolor(WHITE+BLINK);
textbackground(BLUE);
gotoxy(7,18);
cprintf("\n      O.K        ");
delay(10000);
/*goto screen2; */

finish:
getch();
return(0);
}
```

Appendix B

Data Sheets:

JK1545 2-Phase Stepper Motor Driver



Characteristic:

1.DC power input type:24V~50VDC

2.Output current:1.3A-4.5A

3.Mircostepping：1(1.8°)、1/2、1/4、1/8、1/16、1/32、1/64、1/128、1/256

1/5、1/10、1/25、1/50、1/125、1/250

4.Protect form：Overheated protect, lock automatic half current ,error connect protect

5.Dimensions：118mm×76mm×33mm

6.Weight：<300g.

7.Working environment：Temperature-15～40℃ Humidity<90%。

I/O Ports:

:

1、 VCC+ : DC power positive pole

Note:Must guard against exceeding 50V,

so as not to damage the module

2、GND : DC power cathode

3、A+、A- : Stepping motor one winding

4、B+、B- : Stepping motor other winding

5、PUL+、PUL - : Stepping pulse input+5V (Rising edge effective , rising edge duration >10μS)

6、DIR +、DIR- : Stepping motor direction input, voltage level touched off,high towards, low reverse

7、ENA+、ENA-: motor free

NOTE :

1, When ambient temperature is high or working current over 2.7A, fix the module on big metal shell , or use axle flows fan dispels the heat, to make the module run reliably for a long time.

2, Half current automatically: if control machine not send out signal in half second, driver enter half current state of automatically for electricity saving, the phase current of the winding of the electric

3, The fault phase is protected : When the double-phase electrical machinery is connected with driver , users are apt to connect the phase by mistake, thus would damage the driver seriously. The protecting circuit is within this driver, when users connect by mistake, the driver will not be damaged, but the electrical machinery runs abnormally, shake , and output is small.Please check whether the wiring of electrical machinery is a mistake

Switch Choice: ("ON=0, OFF=1")

1、Microstepping choice:

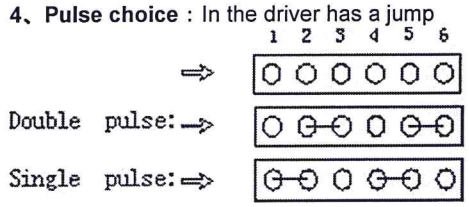
SW5	0	0	0	0	0	0	0	0	1	1	1	1	1	1
SW6	0	1	0	1	0	1	0	1	0	1	0	1	0	1
SW7	0	0	1	1	0	0	1	1	0	0	1	1	0	0
SW8	0	0	0	0	1	1	1	1	0	0	0	0	1	1
Micro	1/2	1/4	1/8	1/16	1/32	1/64	1/128	1/256	1/5	1/10	1/25	1/50	1/125	1/250

2、Current choice :

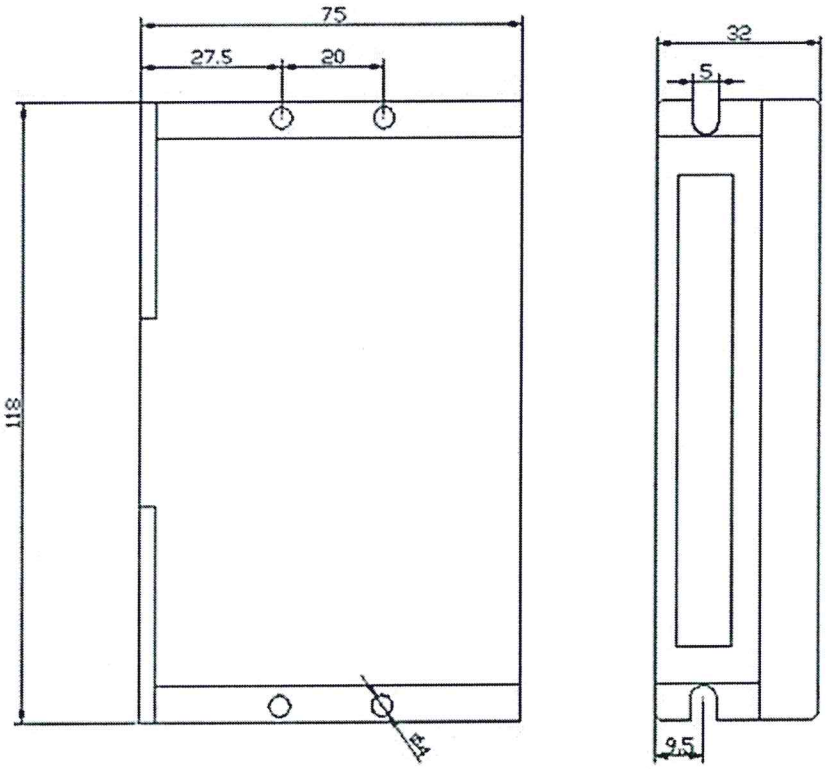
SW1	0	1	0	1	0	1	0	1
SW2	0	0	1	1	0	0	1	1
SW3	0	0	0	0	1	1	1	1
Current (A)	1.3	1.8	2.3	2.7	3.2	3.7	4.2	4.5

3、Full current or half current choice : SW4 : 0=Full current ; 1=half current

4、Pulse choice : In the driver has a jump



5、installation dimension (mm)



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Orientation of Radar Antenna

Tayseer Mustafa Hummaida 1, Abdelrasoul Jabar Alzubaidi 2, Yousif Taha Yousif Elamin 3

1 Post graduate candidate,
2 Sudan University of science and Technology- Engineering College- Electronics Dept- –
3 Electronics Dept. - Faculty of Engineering & Technology - University of Gezira -

Abstract: *A Radar PPI display is considered to display a dummy blip (target) in order to perform orientation procedure on it. Several works have been done in the area of radar antenna orientation and control system using stepper motor control . In order to speed up the data rate, the antennas are required to operate at higher radio frequencies. The increased frequency requires more precise antenna pointing system and the need of pointing control is to counteract the effects of external disturbances which includes wind gust, terrain profile etc. All these factors demand an embedded system engineer to design a more accurate antenna control system. This paper describes the control system engineering principles used in designing, testing and implementing, a control and measurement system on an antenna orientation. The control system is modeled to monitor and control the antenna in the azimuth (Horizontal axis). The system is also stabilized with the help of level sensor.*

Keywords: *Radar, antenna, azimuth, PPI, blip, orientation, embedded system.*

I. Introduction

The antenna azimuth position control system turns the input command in output position. This system is widely used in antennas, robots, and computers disks. In this work the system presented is managed with azimuth antenna. Figure (1) below shows how the system works and how its performance can be improved. The purpose of this system is the input angle to be turned into an output angle of the antenna.

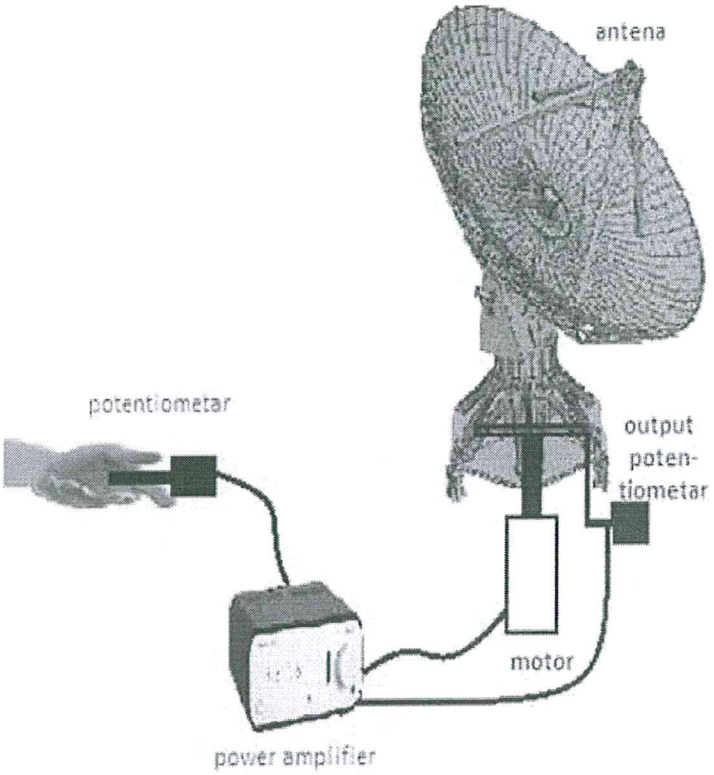


Figure (1) Antenna position control

The antenna control system representation is shown in figure (2) below.

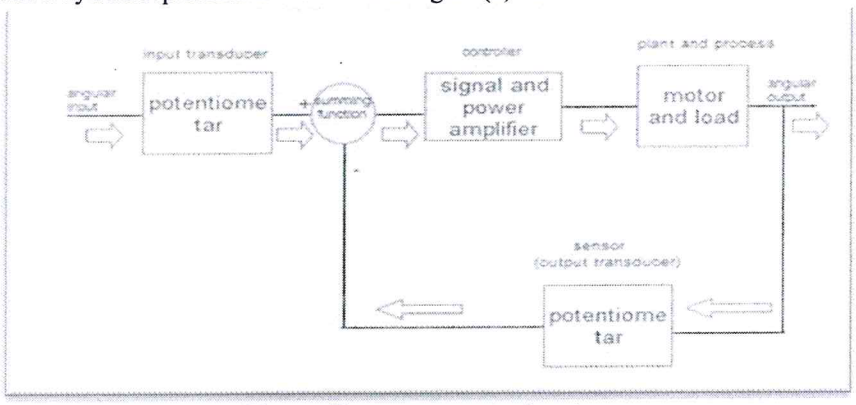


Figure (2) antenna control system

For improving the control system , an approach of micro-stepping control for the step motors based on field programmable gate array (FPGA) is presented after the micro-stepping driving theory of the step motor with a constant torque was discussed deeply. And then the relative control system is schematically designed, mainly includes the internal logic design of the FPGA, the communication interface design of the microcomputer, the design of the power driving circuit, and the design of the interface circuit between the electrical sources. At last, it is verified by some experimental investigations that the control theory and approach presented are corrective, and the control system designed is very good to get a high precision of position control and high control repeatability. Therefore, the technology questions from the producing reality are resolved and the product quality is promoted.

An open loop stepper motor driver using a FPGA is also feasible. The model of the current controller is described and gains of the controller are selected at optimal values. In this design, the FPGA is used to build a high performance open loop driver without using a DSP; furthermore it is compatible with ASICs and mass production methods. The experimental results verify the performance of the driver. In addition, stepper motor controller is used to drive the stepper motor. A Very High Speed Integrated Circuit Hardware Description Language (VHDL) is implemented on SPARATAN Field Programmable Gate Array (FPGA). The Proposed motor controller is a set of Darlington amplifiers thus giving very high precision. Due to high torque of stepper motor, it is capable of handling the big industrial automation system. In this system, a potentiometer technique will be designed to give the control parameter to the FPGA, which in its turn controls the stepper motor.

II. Methodology

This paper describes a stepper motor control algorithm designed using VHDL and implemented in FPGA. The system is capable of controlling the stepper motor in terms of a very small step angle. In addition to this, we can make it to rotate at different speeds, displacement clockwise and anticlockwise directions. Here a potentiometer is used for inputting the control parameter to faithfully control the antenna azimuth angle by rotating the stepper motor clockwise and anticlockwise.

One of the major advantages of the design is its precision. It is user-friendly reduces programming complexity and errors can be easily identified and rectified . The main block diagram is based guiding the signal from Plane Position Indicator of the Radar (PPI) to the FPGA. Figure (3) below shows the block diagram of the system design.

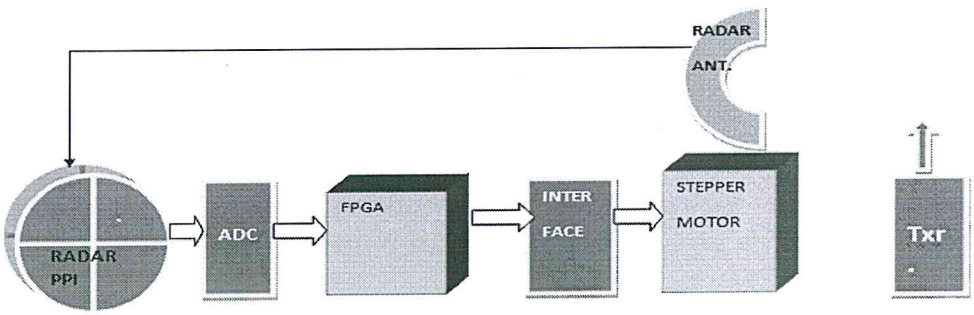


Figure (3) the block diagram of the system

Hardware component

The hardware components for the electronic circuit design are:

Breadboard:

Breadboard (protoboard) is a construction base for a one-of-a-kind electronic circuit, a prototype. Because the solder less breadboard does not require soldering, it is reusable, and thus can be used for temporary prototypes and experimenting with circuit design more easily. A variety of electronic systems may be prototyped by using breadboards.

Potentiometer:

It is used as a means of pointing to the blip on the PPI of the Radar.

ADC8080:

It is used to transform the analog signal from the PPI of the Radar into digital format to be fed to the FPGA for processing.

HD74LS373 Latching IC:

The HD74LS373 is eight bit is register I/O mapped used as a buffer, which stores signals for future use. Different types of latches are available HD74LS373 octal D-type transparent latch will be used in this system. This type of latch is suitable for driving high capacitive and impedance loads.

ULN 2893A Darlington IC:

The ULN2803A is a high-voltage, high-current Darlington transistor array. The device consists of eight NPN Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of each Darlington pair is 500 mA. .The Darlington pairs may be connected in parallel for higher current capability.

Lab link cable:

The lab link cables are used as a connection means in the circuit right from the PPI of the Radar up to the stepper motor.

Stepper motor:

A stepper motor is used for the procedure of orientation of the antenna of the Radar .The number of steps of the stepper motor is (200 steps / revolution). Equation (1) gives the value of the step angle of the stepper motor.

$$\text{Step angle} = \frac{\text{One revolution}}{200} = \frac{360^0}{200} = 1.8 \text{ Degree} \quad \text{---------- (1)}$$

III. Algorithm

The algorithm is based on supplying the FPGA through the ADC with the azimuth angle appeared on the PPI of the Radar in the digital format .The FPGA in its turn processes the data and issues a correction command to the stepper motor in order to align the antenna to the geographical north (0^0) . The orientation procedure of the Radar antenna is as follows;

.. The transmitter issues a signal.
.. The PPI of the Radar displays the transmitter signal as a dummy target on the PPI.
.. A potentiometer points to the blip (target) to convey the azimuth angle.
.. The ADC transforms the DC voltage into digital format.
.. The FPGA processes the digital data.
.. The FPGA issues correction command to the stepper motor through the interface.
.. The stepper motor aligns the antenna to the geographical north (0^0).

VHDL programming language is used for programming the FPGA by the computer the algorithm is:

Start

Initialization:

... Program port (A1) of FPGA as input.
... Program port (A2) of FPGA as output.
--- Put transmitter mode to (OFF).
--- Adjust the plane position indicator (PPI) of the Radar to the geographical north (0^0).

--- Clear output to stepper motor.

Processing:
--- Put transmitter mode to (ON).
---- Call orientation subroutine.
End
Orientation subroutine:
Blip detection:
--- Observe the blip on the PPI of the Radar.
... Move the slide of the potentiometer to coincide with the blip on the PPI.
... Check the incoming azimuth value of the blip.
--- If the azimuth value equals zero, then go to terminate the subroutine.
--- If the azimuth value does not equal zero, then go to antenna position correction.
... Go to blip detection.

Antenna position correction:
... If the azimuth value is positive, then rotate the stepper motor one-step anticlockwise.
... If the azimuth value is negative, then rotate the stepper motor one-step clockwise.
--- Go to blip detection.
Terminate:
Return.

IV. Results

A transmitter tuned to the Radar receiver frequency is used to generate a blip (dummy target) on the PPI display of the Radar. when applying the algorithm in paragraph (III) above, we observe the location of the blip on the PPI .Based on the blip azimuth angle, the program in the FPGA performs the alignment of the antenna with the blip appearance on the PPI of the Radar .The alignment processing continues till we get the antenna exactly heading to the geographical north (0 Degrees). Each step movement of the stepper motor makes an antenna azimuth angle correction of (1.8 Degrees) .A mechanical gearing mechanism is implemented to enhance the stepper motor angle resolution up to of (0.18 Degrees). Table (1) below shows the results obtained from the generation of four different dummy blips (targets) on the PPI display of the Radar and performing antenna orientation procedure on them

Table (1) the results obtained from generating a blip (target) on the PPI display of the Radar

Blip azimuth angle on PPI (Degrees)	No. of steps of stepper motor	Alignment result
$+18^0$ East	100 anticlockwise	Geographical north (0^0)
-9^0 West	50 clockwise	Geographical north (0^0)
$+27^0$ East	150 anticlockwise	Geographical north (0^0)
-13.5^0 West	75 clockwise	Geographical north (0^0)

Note: The alignment (orientation) can be done by pointing towards (East, South, and West) As well.

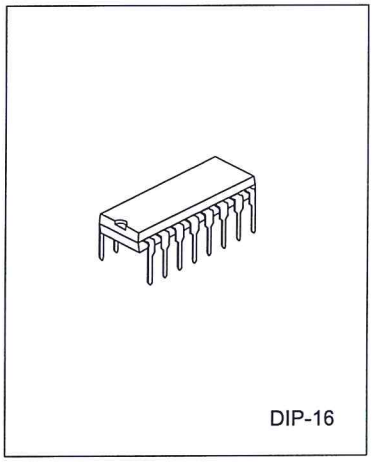
V. Conclusion

The functionality of the design starts with activating a transmitter tuned to the Radar frequency. A dummy blip (target) appears on the PPI display of the Radar. Any antenna azimuth angle deviation from the geographical north will be subjected to correction procedure. Based on the blip appearance on the PPI, the FPGA program performs the correction by commanding the stepper motor to rotate clockwise or anticlockwise. The processing outcome is to put both the antenna and the PPI display on (0^0). The alignment procedure (orientation) makes us avoiding azimuth data capture errors by the Radar.

References

[1]. Mr.N.Sai Pavan, Mr.Ramavenkateswaran.N: MODELLING OF TH STABILIZATIONAND TRACKING CONTROL SYSTEM FOR ANTENNA, International Journal Of Advanced Research In Computer And Communication Engineering, June 2014.
[2]. Boban Temelkovskia And Jugoslav Achkoskia "Modeling And Simulation Of Antenna Azimuth Position Control System "International Journal Of Multidisciplinary And Current Research,2014.
[3]. Xiaodong Zhang, Junjun He, And Chunlei Sheng, "Anapproach Of Micro-Stepping Control For The Step Motors Based On FPGA," IEEE International Conference On Industrial Technology, Pp. 125 - 130, Dec. 2005.
[4]. Ngoc Quy Le1 And Jae Wook Jeon2" An Open-Loop Stepper Motor Driver Based On FPGA" International Conference On Control, Automation And Systems 2007Oct. 17-20, 2007 In COEX, Seoul, Korea
[5]. Arvind Kumar1, Mrs. M. Valarmathi2" High Precision Stepper Motor Controller Implementation On FPGA With GUI On Labview"International Journal Of Advanced Research In Electrical, Electronics And Instrumentation Engineering Vol. 2, Issue 4, April 2013

HIGH VOLTAGE AND HIGH CURRENT DARLINGTON TRANSISTOR ARRAY



DESCRIPTION

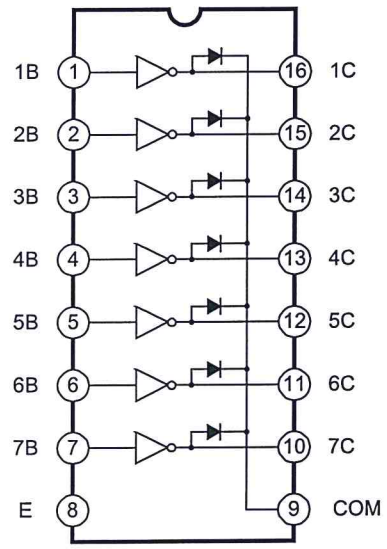
The ULN2003 is a monolithic high voltage and high current Darlington transistor arrays. It consists of seven NPN darlington pairs that features high-voltage outputs with common-cathode clamp diode for switching inductive loads. The collector-current rating of a single darlington pair is 500mA. The darlington pairs may be parrlleled for higher current capability. Applications include relay drivers,hammer drivers, lampdrivers,display drivers(LED gas discharge),line drivers, and logic buffers.

The ULN2003 has a 2.7kΩ series base resistor for each darlington pair for operation directly with TTL or 5V CMOS devices.

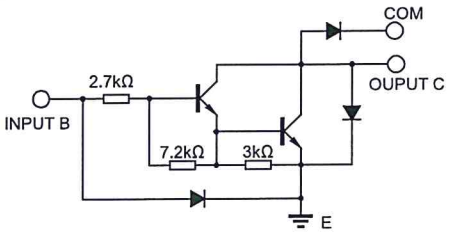
FEATURES

* 500mA rated collector current(Single output)
* High-voltage outputs: 50V
* Inputs compatibale with various types of logic.
* Relay driver application

LOGIC DIAGRAM



SCHEMATIC(EACH DARLINGTON PAIR)



ABSOLUTE MAXIMUM RATINGS(Ta=25°C)

Characteristic	Symbol	Value	Unit
Colletor-Emitter Voltage	V_{CE}	50	V
Input Voltage	V_I	30	A
Peak Collector Current	I_O	500	mA
Total Emitter-terminal	I_{OK}	500	mA
Power Dissipation	Pd	950 Tamb=25°C 495 Tamb<85°C	mW mW
Operating Temperature	Topr	-20~ +85	°C
Storage Temperature	Tstg	-65 ~ +150	°C

Note: All volatge values are with repect to the emitter/substrate terminal E, unless otherwise noted.

ELECTRICAL CHARACTERISTICS(Ta=25°C,unless otherwise specified)

Characteristic	Test Figure	Symbol	Test Conditions	Min	Typ	Max	Units
On-state Input Voltage	6	$V_{I(ON)}$	V_{CE}=2V,Ic=200mA			2.4	V
			V_{CE}=2V,Ic=250mA			2.7	
			V_{CE}=2V,Ic=300mA			3	
Collector-Emitter Saturation Voltage	5	$V_{CE(SAT)}$	I_I=250μA,Ic=100mA		0.9	1.1	V
			I_I=350μA,Ic=200mA		1	1.3	
			I_I=500μA,Ic=350mA		1.2	1.6	
Collector Cutoff Current	1	I_{CEX}	V_{CE}=50V,I_I=0			50	μA
	2		V_{CE}=50V,I_I=0,Ta=70°C			100	
Clamp Forward Voltage	8	V_F	I_F=350mA		1.7	2	V
Off-state Input Current	3	$I_{I(OFF)}$	V_{CE}=50V,Ic=500mA, Ta=70°C	50	65		μA
Input Current	4	I_I	V_I=3.85V		0.95	1.35	mA
Clamp Reverse Current	7	I_R	V_R=50V			50	μA
			V_R=50V, Ta=70°C			100	
Input Capacitance	--	C_I	V_I=0,f=1MHz		15	25	pF
Propagation delay time, low-to-high-level output	9	t_{PLH}			0.25	1	μs
Propagation delay time, high-to-low-level output	9	t_{PHL}			0.25	1	μs
High-level output Voltage after switching	10	V_{OH}	Vs=50V,Io=300mA	Vs-20			mV

TEST CIRCUITS

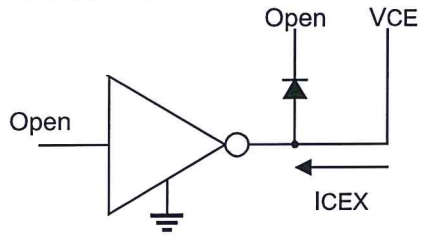


Figure 1 ICEX Test Circuit

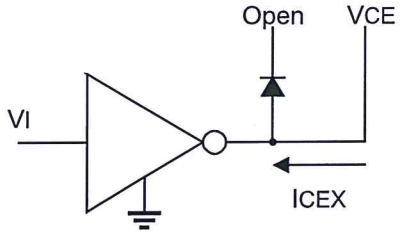


Figure 2 ICEX Test Circuit

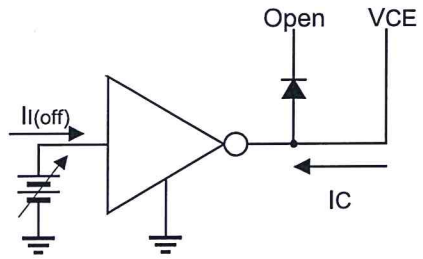


Figure 3 II(off) Test Circuit

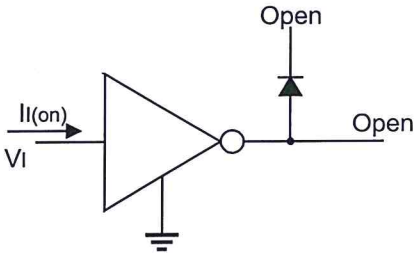
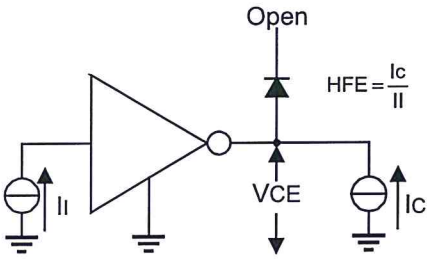


Figure 4 II(on) Test Circuit



Note: II is fixed for measuring VCE(sat),variable for measuring HFE.

Figure 5 HFE,VCE(sat) Test Circuit

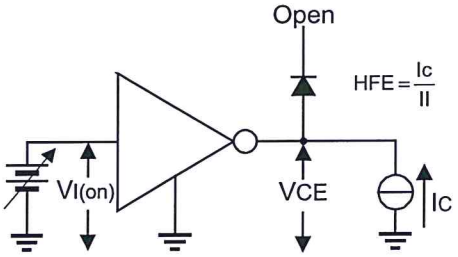


Figure 6 VI(on) Test Circuit

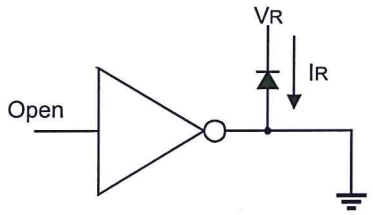


Figure 7 IR Test Circuit

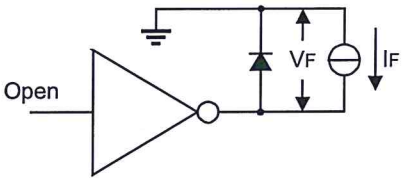


Figure 8 VF Test Circuit

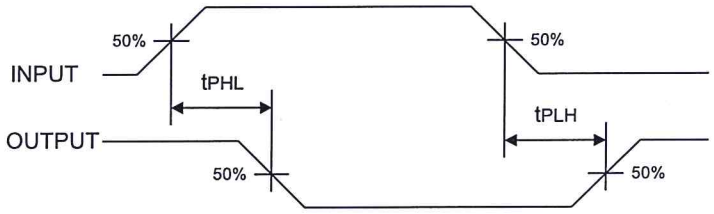
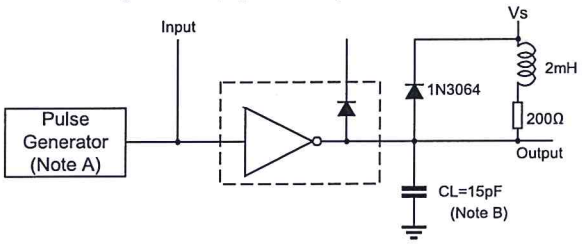
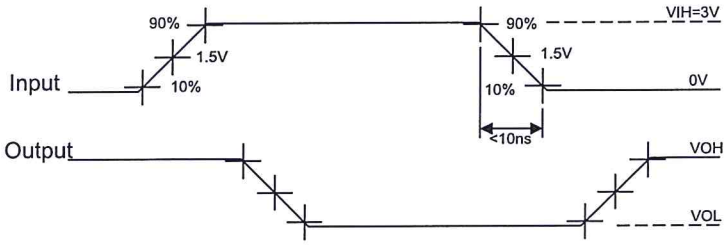


Figure 9. Propagation Delay Time Waveforms





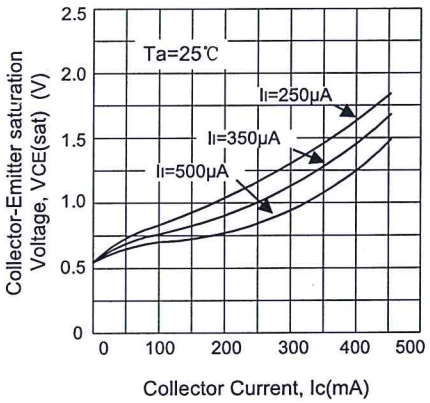
Note: A. The Pulse generatoe has the following characteristics: PRR=12.5kHz, Zo=50Ω

B. CL includes proble and jig capacitance.

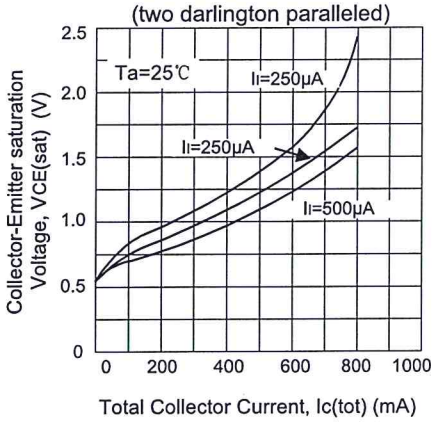
Figure 10. Latch-up Test Circuit and Voltage Waveforms

TYPICAL PERFORMANCE CHARACTERISTICS

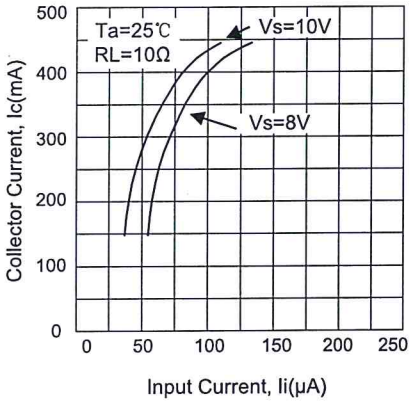
Collector-Emitter saturation Voltage vs. Collector Current



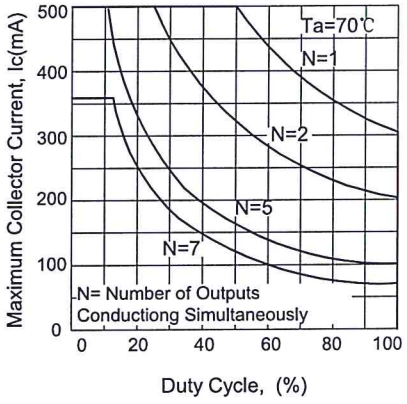
Collector-Emitter saturation Voltage vs. Total Collector Current (two darlington paralleled)



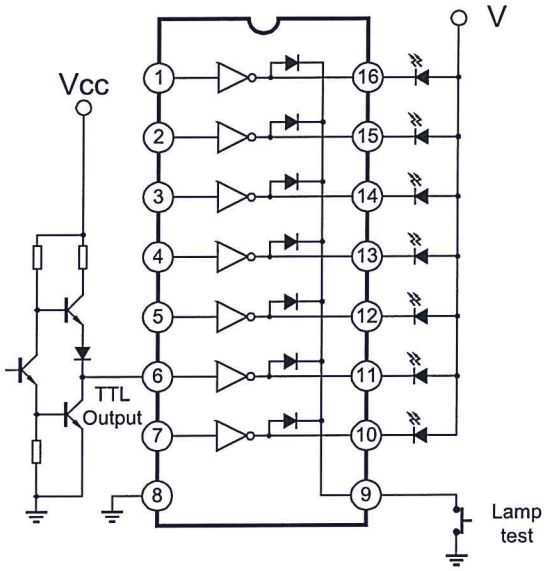
Collector Current Vs. Input Current



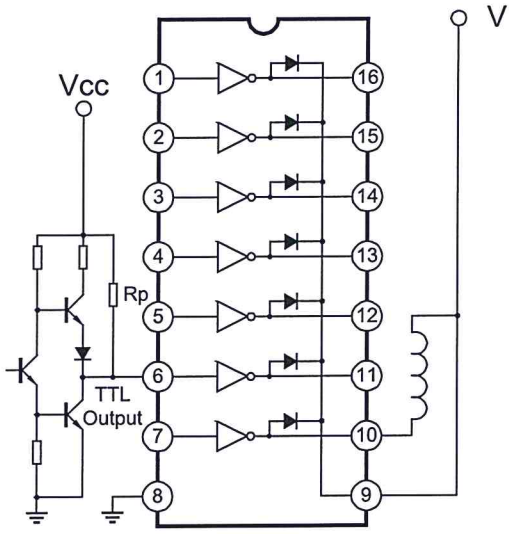
Maximum Collector Current Vs. Duty cycle



TYPICAL APPLICATION CIRCUIT



TTL to Load



Use of pullup Resistor to increase drive Current

October 1999

National Semiconductor

ADC0808/ADC0809
8-Bit µP Compatible A/D Converters with 8-Channel Multiplexer

General Description

The ADC0808, ADC0809 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 8-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 8-channel multiplexer can directly access any of 8-single-ended analog signals.

The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE® outputs.

The design of the ADC0808, ADC0809 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0808, ADC0809 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications from process and machine control to consumer and automotive applications. For 16-channel multiplexer with common output (sample/hold port) see ADC0816 data sheet. (See AN-247 for more information.)

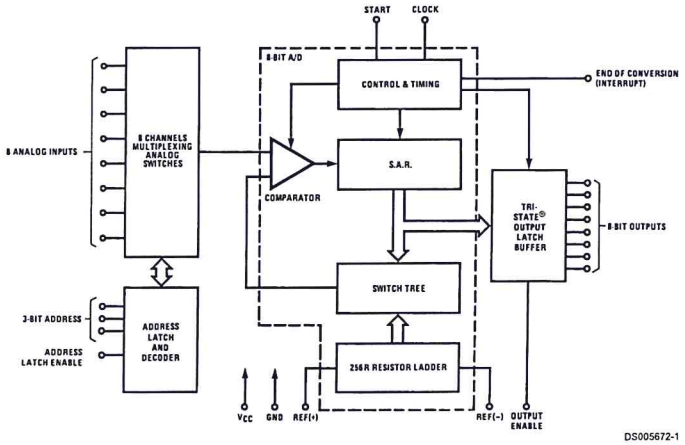
Features

- Easy interface to all microprocessors
- Operates ratiometrically or with 5 V_{DC} or analog span adjusted voltage reference
- No zero or full-scale adjust required
- 8-channel multiplexer with address logic
- 0V to 5V input range with single 5V power supply
- Outputs meet TTL voltage level specifications
- Standard hermetic or molded 28-pin DIP package
- 28-pin molded chip carrier package
- ADC0808 equivalent to MM74C949
- ADC0809 equivalent to MM74C949-1

Key Specifications

■ Resolution	8 Bits
■ Total Unadjusted Error	±½ LSB and ±1 LSB
■ Single Supply	5 V_{DC}
■ Low Power	15 mW
■ Conversion Time	100 µs

Block Diagram

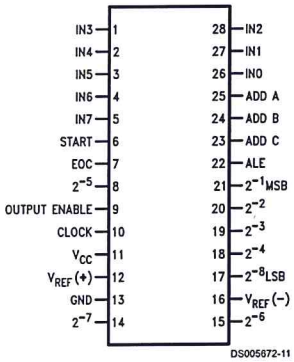


See Ordering Information

TRI-STATE® is a registered trademark of National Semiconductor Corp.

Connection Diagrams

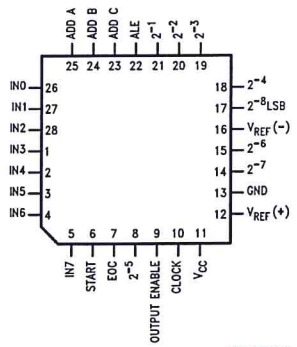
Dual-In-Line Package



DS005672-11

Order Number ADC0808CCN or ADC0809CCN
See NS Package J28A or N28A

Molded Chip Carrier Package



DS005672-12

Order Number ADC0808CCV or ADC0809CCV
See NS Package V28A

Ordering Information

TEMPERATURE RANGE		−40°C to +85°C			−55°C to +125°C
Error	±½ LSB Unadjusted	ADC0808CCN	ADC0808CCV	ADC0808CCJ	ADC0808CJ
	±1 LSB Unadjusted	ADC0809CCN	ADC0809CCV		
Package Outline		N28A Molded DIP	V28A Molded Chip Carrier	J28A Ceramic DIP	J28A Ceramic DIP

Absolute Maximum Ratings (Notes 2, 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage at Any Pin Except Control Inputs	−0.3V to (V_{CC}+0.3V)
Voltage at Control Inputs (START, OE, CLOCK, ALE, ADD A, ADD B, ADD C)	−0.3V to +15V
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A=25°C	875 mW
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Molded Chip Carrier Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
ESD Susceptibility (Note 8)	400V

Operating Conditions (Notes 1, 2)

Temperature Range (Note 1)	$T_{MIN} \le T_A \le T_{MAX}$
ADC0808CCN,ADC0809CCN	−40°C≤T_A≤+85°C
ADC0808CCV, ADC0809CCV	−40°C ≤ T_A ≤ +85°C
Range of V_{CC} (Note 1)	4.5 V_{DC} to 6.0 V_{DC}

Electrical Characteristics

Converter Specifications: V_{CC}=5 V_{DC}=V_{REF+}, $V_{REF(-)}$=GND, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK}=640 kHz unless otherwise stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	ADC0808					
	Total Unadjusted Error	25°C			±½	LSB
	(Note 5)	T_{MIN} to T_{MAX}			±¾	LSB
	ADC0809					
	Total Unadjusted Error	0°C to 70°C			±1	LSB
	(Note 5)	T_{MIN} to T_{MAX}			±1¼	LSB
	Input Resistance	From Ref(+) to Ref(−)	1.0	2.5		kΩ
	Analog Input Voltage Range	(Note 4) V(+) or V(−)	GND−0.10		V_{CC}+0.10	V_{DC}
$V_{REF(+)}$	Voltage, Top of Ladder	Measured at Ref(+)		V_{CC}	V_{CC}+0.1	V
$\frac{V_{REF(+)}+V_{REF(-)}}{2}$	Voltage, Center of Ladder		V_{CC}/2-0.1	V_{CC}/2	V_{CC}/2+0.1	V
$V_{REF(-)}$	Voltage, Bottom of Ladder	Measured at Ref(−)	−0.1	0		V
I_{IN}	Comparator Input Current	f_c=640 kHz, (Note 6)	−2	±0.5	2	μA

Electrical Characteristics

Digital Levels and DC Specifications: ADC0808CCN, ADC0808CCV, ADC0809CCN and ADC0809CCV, 4.75≤V_{CC}≤5.25V, −40°C≤T_A≤+85°C unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ANALOG MULTIPLEXER						
$I_{OFF(+)}$	OFF Channel Leakage Current	V_{CC}=5V, V_{IN}=5V,				
		T_A=25°C		10	200	nA
		T_{MIN} to T_{MAX}			1.0	μA
$I_{OFF(-)}$	OFF Channel Leakage Current	V_{CC}=5V, V_{IN}=0,				
		T_A=25°C	−200	−10		nA
		T_{MIN} to T_{MAX}	−1.0			μA
CONTROL INPUTS						
$V_{IN(1)}$	Logical "1" Input Voltage		V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage				1.5	V
$I_{IN(1)}$	Logical "1" Input Current (The Control Inputs)	V_{IN}=15V			1.0	μA
$I_{IN(0)}$	Logical "0" Input Current (The Control Inputs)	V_{IN}=0	−1.0			μA
I_{CC}	Supply Current	f_{CLK}=640 kHz		0.3	3.0	mA

Electrical Characteristics (Continued)

Digital Levels and DC Specifications: ADC0808CCN, ADC0808CCV, ADC0809CCN and ADC0809CCV, $4.75 \le V_{CC} \le 5.25V$, $-40^{\circ}C \le T_A \le +85^{\circ}C$ unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DATA OUTPUTS AND EOC (INTERRUPT)						
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 4.75V I_{OUT} = −360µA I_{OUT} = −10µA		 **2.4** **4.5**		 V(min) V(min)
$V_{OUT(0)}$	Logical "0" Output Voltage	I_O=1.6 mA			0.45	V
$V_{OUT(0)}$	Logical "0" Output Voltage EOC	I_O=1.2 mA			0.45	V
I_{OUT}	TRI-STATE Output Current	V_O=5V V_O=0	 −3		3	µA µA

Electrical Characteristics

Timing Specifications $V_{CC}=V_{REF(+)}$=5V, $V_{REF(-)}$=GND, $t_r=t_f$=20 ns and T_A=25°C unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{WS}	Minimum Start Pulse Width	(*Figure 5*)		100	200	ns
t_{WALE}	Minimum ALE Pulse Width	(*Figure 5*)		100	200	ns
t_s	Minimum Address Set-Up Time	(*Figure 5*)		25	50	ns
t_H	Minimum Address Hold Time	(*Figure 5*)		25	50	ns
t_D	Analog MUX Delay Time From ALE	R_S=0Ω (*Figure 5*)		1	2.5	µs
t_{H1}, t_{H0}	OE Control to Q Logic State	C_L=50 pF, R_L=10k (*Figure 8*)		125	250	ns
t_{1H}, t_{0H}	OE Control to Hi-Z	C_L=10 pF, R_L=10k (*Figure 8*)		125	250	ns
t_c	Conversion Time	f_c=640 kHz, (*Figure 5*) (Note 7)	90	100	116	µs
f_c	Clock Frequency		10	640	1280	kHz
t_{EOC}	EOC Delay Time	(*Figure 5*)	0		8+2 µS	Clock Periods
C_{IN}	Input Capacitance	At Control Inputs		10	15	pF
C_{OUT}	TRI-STATE Output Capacitance	At TRI-STATE Outputs		10	15	pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to GND, unless othewise specified.

Note 3: A zener diode exists, internally, from V_{CC} to GND and has a typical breakdown voltage of 7 V_{DC}.

Note 4: Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC}n supply. The spec allows 100 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 100 mV, the output code will be correct. To achieve an absolute $0V_{DC}$ to $5V_{DC}$ input voltage range will therefore require a minimum supply voltage of 4.900 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors. See *Figure 3*. None of these A/Ds requires a zero or full-scale adjust. However, if an all zero code is desired for an analog input other than 0.0V, or if a narrow full-scale span exists (for example: 0.5V to 4.5V full-scale) the reference voltages can be adjusted to achieve this. See *Figure 13*.

Note 6: Comparator input current is a bias current into or out of the chopper stabilized comparator. The bias current varies directly with clock frequency and has little temperature dependence (*Figure 6*). See paragraph 4.0.

Note 7: The outputs of the data register are updated one clock cycle before the rising edge of EOC.

Note 8: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Functional Description

Multiplexer. The device contains an 8-channel single-ended analog signal multiplexer. A particular input channel is selected by using the address decoder. *Table 1* shows the input states for the address lines to select any channel. The address is latched into the decoder on the low-to-high transition of the address latch enable signal.

TABLE 1.

SELECTED ANALOG CHANNEL	ADDRESS LINE		
	C	B	A
IN0	L	L	L
IN1	L	L	H
IN2	L	H	L
IN3	L	H	H
IN4	H	L	L
IN5	H	L	H
IN6	H	H	L
IN7	H	H	H

CONVERTER CHARACTERISTICS

The Converter

The heart of this single chip data acquisition system is its 8-bit analog-to-digital converter. The converter is designed to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into 3 major sections: the 256R ladder network, the successive approximation register, and the comparator. The converter's digital outputs are positive true.

The 256R ladder network approach (*Figure 1*) was chosen over the conventional R/2R ladder because of its inherent monotonicity, which guarantees no missing digital codes. Monotonicity is particularly important in closed loop feedback control systems. A non-monotonic relationship can cause oscillations that will be catastrophic for the system. Additionally, the 256R network does not cause load variations on the reference voltage.

The bottom resistor and the top resistor of the ladder network in *Figure 1* are not the same value as the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full-scale points of the transfer curve. The first output transition occurs when the analog signal has reached +½ LSB and succeeding output transitions occur every 1 LSB later up to full-scale.

The successive approximation register (SAR) performs 8 iterations to approximate the input voltage. For any SAR type converter, n-iterations are required for an n-bit converter. *Figure 2* shows a typical example of a 3-bit converter. In the ADC0808, ADC0809, the approximation technique is extended to 8 bits using the 256R network.

The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start conversion (SC) pulse. The conversion is begun on the falling edge of the start conversion pulse. A conversion in process will be interrupted by receipt of a new start conversion pulse. Continuous conversion may be accomplished by tying the end-of-conversion (EOC) output to the SC input. If used in this mode, an external start conversion pulse should be applied after power up. End-of-conversion will go low between 0 and 8 clock pulses after the rising edge of start conversion.

The most important section of the A/D converter is the comparator. It is this section which is responsible for the ultimate accuracy of the entire converter. It is also the comparator drift which has the greatest influence on the repeatability of the device. A chopper-stabilized comparator provides the most effective method of satisfying all the converter requirements.

The chopper-stabilized comparator converts the DC input signal into an AC signal. This signal is then fed through a high gain AC amplifier and has the DC level restored. This technique limits the drift component of the amplifier since the drift is a DC component which is not passed by the AC amplifier. This makes the entire A/D converter extremely insensitive to temperature, long term drift and input offset errors.

Figure 4 shows a typical error curve for the ADC0808 as measured using the procedures outlined in AN-179.

Functional Description (Continued)

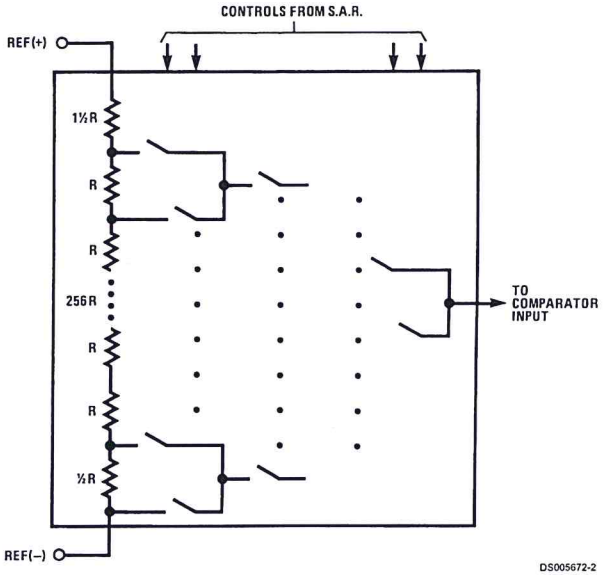


FIGURE 1. Resistor Ladder and Switch Tree

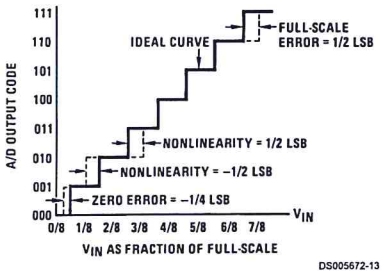


FIGURE 2. 3-Bit A/D Transfer Curve

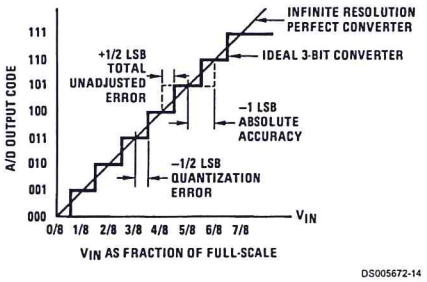


FIGURE 3. 3-Bit A/D Absolute Accuracy Curve

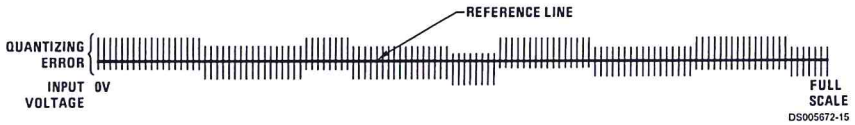


FIGURE 4. Typical Error Curve

Timing Diagram

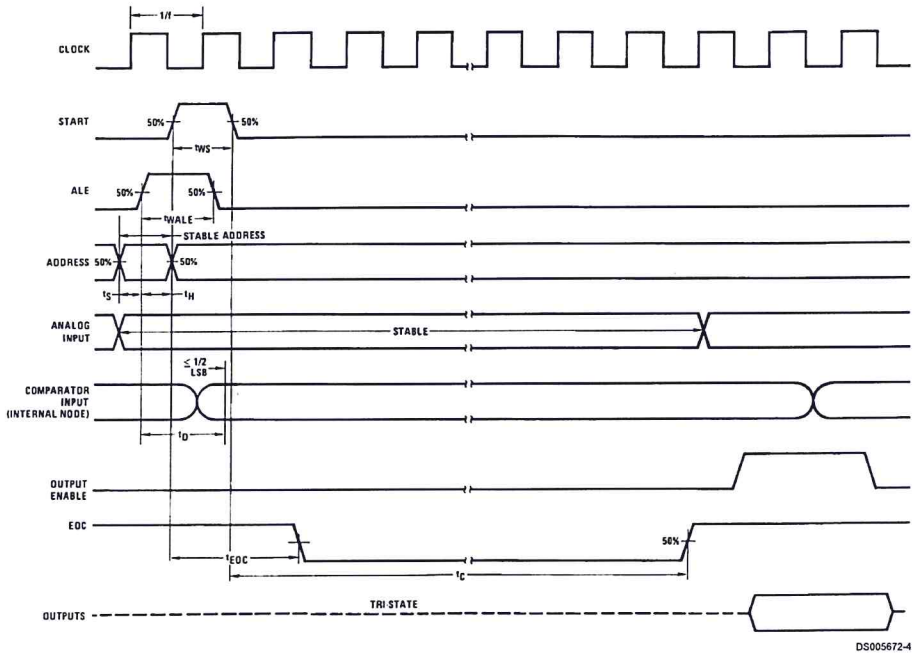


FIGURE 5.

Typical Performance Characteristics

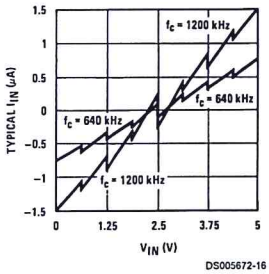


FIGURE 6. Comparator I_{IN} vs V_{IN} (V_{CC}=V_{REF}=5V)

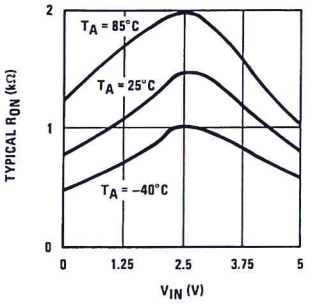


FIGURE 7. Multiplexer R_{ON} vs V_{IN} (V_{CC}=V_{REF}=5V)

TRI-STATE Test Circuits and Timing Diagrams

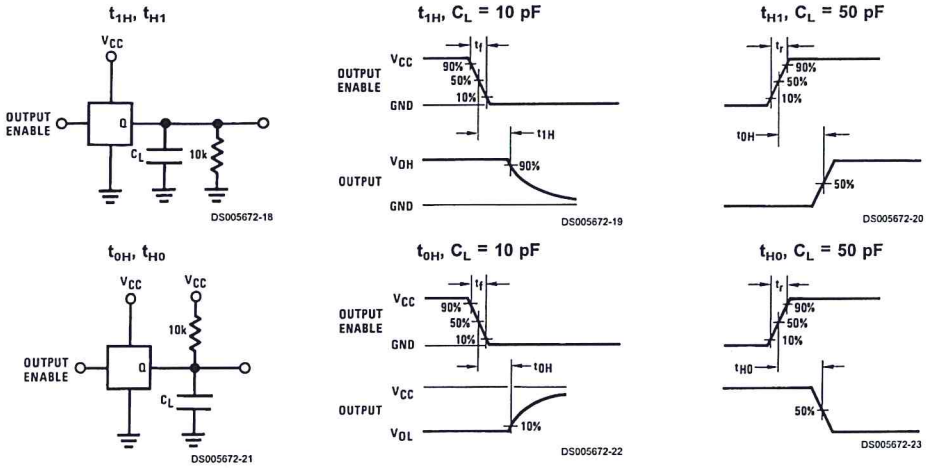


FIGURE 8.

Applications Information

OPERATION

1.0 RATIOMETRIC CONVERSION

The ADC0808, ADC0809 is designed as a complete Data Acquisition System (DAS) for ratiometric conversion systems. In ratiometric systems, the physical variable being measured is expressed as a percentage of full-scale which is not necessarily related to an absolute standard. The voltage input to the ADC0808 is expressed by the equation

$$\frac{V_{IN}}{V_{fs}-V_Z}=\frac{D_X}{D_{MAX}-D_{MIN}} \qquad (1)$$

V_{IN}=Input voltage into the ADC0808

V_{fs}=Full-scale voltage

V_Z=Zero voltage

D_X=Data point being measured

D_{MAX}=Maximum data limit

D_{MIN}=Minimum data limit

A good example of a ratiometric transducer is a potentiometer used as a position sensor. The position of the wiper is directly proportional to the output voltage which is a ratio of the full-scale voltage across it. Since the data is represented as a proportion of full-scale, reference requirements are greatly reduced, eliminating a large source of error and cost for many applications. A major advantage of the ADC0808, ADC0809 is that the input voltage range is equal to the supply range so the transducers can be connected directly across the supply and their outputs connected directly into the multiplexer inputs, (*Figure 9*).

Ratiometric transducers such as potentiometers, strain gauges, thermistor bridges, pressure transducers, etc., are suitable for measuring proportional relationships; however, many types of measurements must be referred to an absolute standard such as voltage or current. This means a sys-

Applications Information (Continued)

tem reference must be used which relates the full-scale voltage to the standard volt. For example, if $V_{CC}=V_{REF}=5.12V$, then the full-scale range is divided into 256 standard steps. The smallest standard step is 1 LSB which is then 20 mV.

2.0 RESISTOR LADDER LIMITATIONS

The voltages from the resistor ladder are compared to the selected into 8 times in a conversion. These voltages are coupled to the comparator via an analog switch tree which is referenced to the supply. The voltages at the top, center and bottom of the ladder must be controlled to maintain proper operation.

The top of the ladder, Ref(+), should not be more positive than the supply, and the bottom of the ladder, Ref(−), should not be more negative than ground. The center of the ladder voltage must also be near the center of the supply because the analog switch tree changes from N-channel switches to P-channel switches. These limitations are automatically satisfied in ratiometric systems and can be easily met in ground referenced systems.

Figure 10 shows a ground referenced system with a separate supply and reference. In this system, the supply must be trimmed to match the reference voltage. For instance, if a 5.12V is used, the supply should be adjusted to the same voltage within 0.1V.

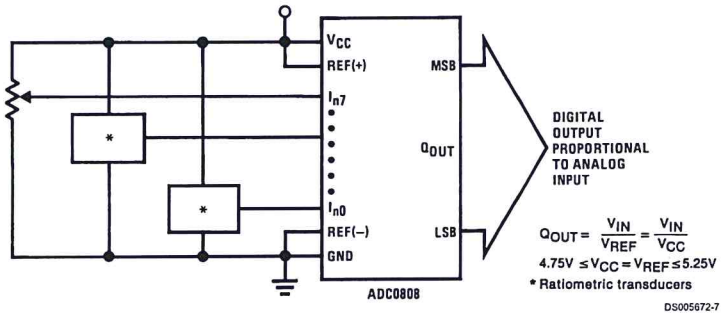
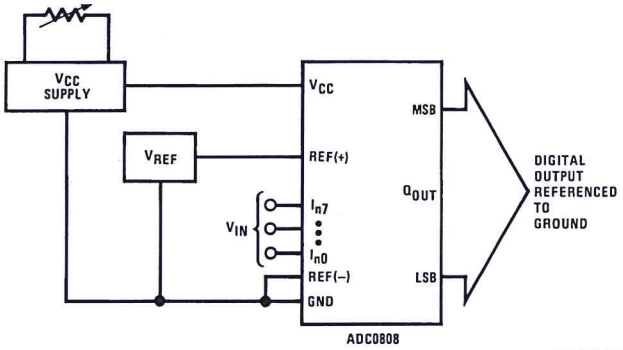


FIGURE 9. Ratiometric Conversion System

The ADC0808 needs less than a milliamp of supply current so developing the supply from the reference is readily accomplished. In *Figure 11* a ground referenced system is shown which generates the supply from the reference. The buffer shown can be an op amp of sufficient drive to supply the milliamp of supply current and the desired bus drive, or if a capacitive bus is driven by the outputs a large capacitor will supply the transient supply current as seen in *Figure 12*. The LM301 is overcompensated to insure stability when loaded by the 10 µF output capacitor.

The top and bottom ladder voltages cannot exceed V_{CC} and ground, respectively, but they can be symmetrically less than V_{CC} and greater than ground. The center of the ladder voltage should always be near the center of the supply. The sensitivity of the converter can be increased, (i.e., size of the LSB steps decreased) by using a symmetrical reference system. In *Figure 13*, a 2.5V reference is symmetrically centered about $V_{CC}/2$ since the same current flows in identical resistors. This system with a 2.5V reference allows the LSB bit to be half the size of a 5V reference system.

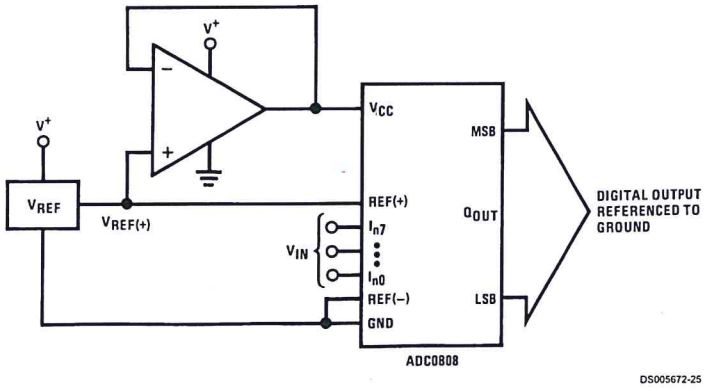
Applications Information (Continued)



$$Q_{OUT} = \frac{V_{IN}}{V_{REF}}$$

$4.75V \leq V_{CC} = V_{REF} \leq 5.25V$

FIGURE 10. Ground Referenced Conversion System Using Trimmed Supply



$$Q_{OUT} = \frac{V_{IN}}{V_{REF}}$$

$4.75V \leq V_{CC} = V_{REF} \leq 5.25V$

FIGURE 11. Ground Referenced Conversion System with Reference Generating V_{CC} Supply

Applications Information (Continued)

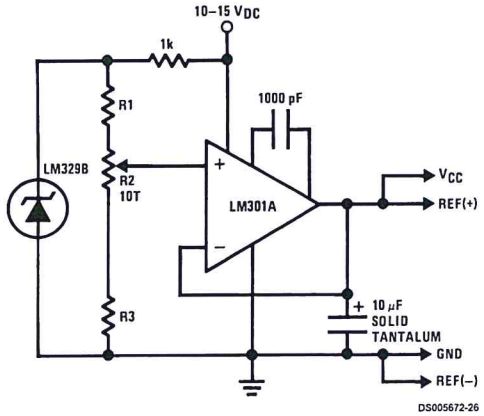
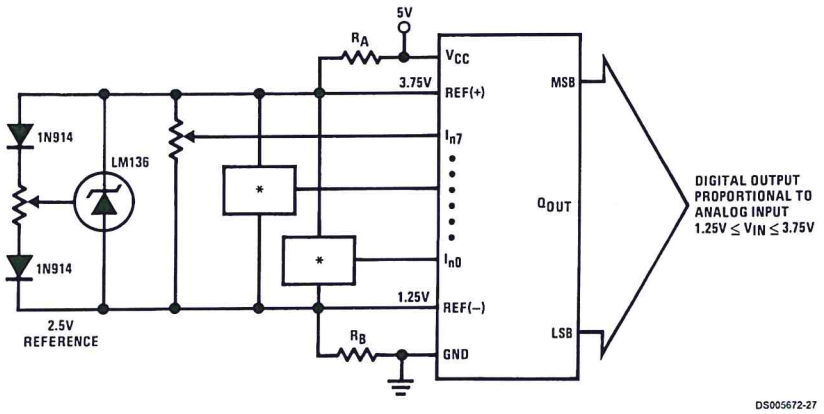


FIGURE 12. Typical Reference and Supply Circuit



$R_A=R_B$

*Ratiometric transducers

FIGURE 13. Symmetrically Centered Reference

3.0 CONVERTER EQUATIONS

The transition between adjacent codes N and N+1 is given by:

$$V_{IN}=\left\{(V_{REF(+)}-V_{REF(-)})\left[\frac{N}{256}+\frac{1}{512}\right]\pm V_{TUE}\right\}+V_{REF(-)} \quad (2)$$

The center of an output code N is given by:

$$V_{IN}\left\{(V_{REF(+)}-V_{REF(-)})\left[\frac{N}{256}\right]\pm V_{TUE}\right\}+V_{REF(-)} \quad (3)$$

The output code N for an arbitrary input are the integers within the range:

$$N=\frac{V_{IN}-V_{REF(-)}}{V_{REF(+)}-V_{REF(-)}}\times 256\pm \text{Absolute Accuracy} \quad (4)$$

Where: V_{IN}=Voltage at comparator input
$V_{REF(+)}$=Voltage at Ref(+)
$V_{REF(-)}$=Voltage at Ref(−)
V_{TUE}=Total unadjusted error voltage (typically $V_{REF(+)}\div 512$)

Applications Information (Continued)

4.0 ANALOG COMPARATOR INPUTS

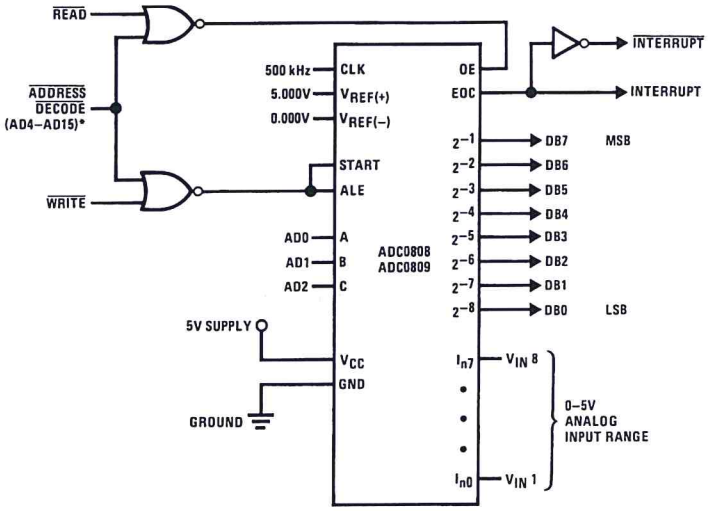
The dynamic comparator input current is caused by the periodic switching of on-chip stray capacitances. These are connected alternately to the output of the resistor ladder/switch tree network and to the comparator input as part of the operation of the chopper stabilized comparator.

The average value of the comparator input current varies directly with clock frequency and with V_{IN} as shown in *Figure 6*.

If no filter capacitors are used at the analog inputs and the signal source impedances are low, the comparator input current should not introduce converter errors, as the transient created by the capacitance discharge will die out before the comparator output is strobed.

If input filter capacitors are desired for noise reduction and signal conditioning they will tend to average out the dynamic comparator input current. It will then take on the characteristics of a DC bias current whose effect can be predicted conventionally.

Typical Application

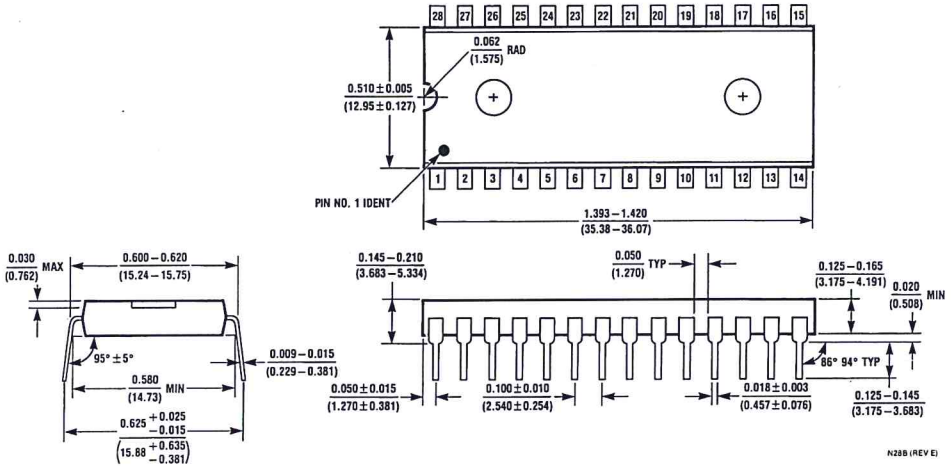


*Address latches needed for 8085 and SC/MP interfacing the ADC0808 to a microprocessor

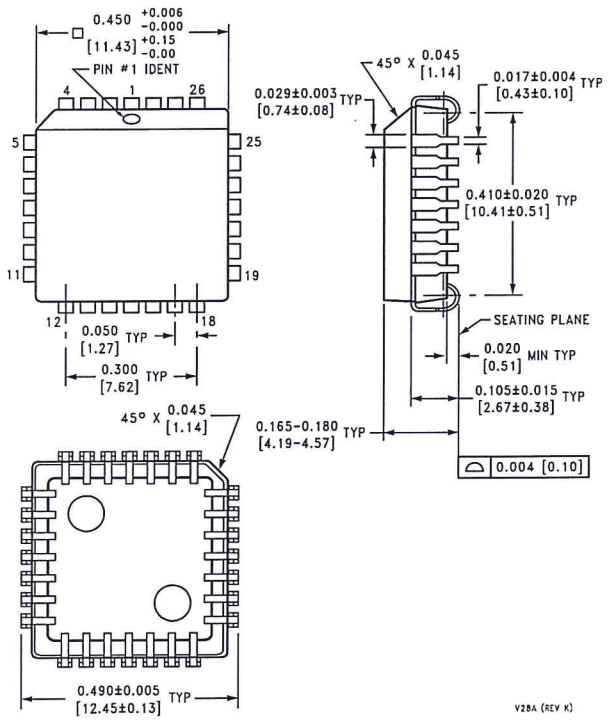
TABLE 2. Microprocessor Interface Table

PROCESSOR	READ	WRITE	INTERRUPT (COMMENT)
8080	MEMR	MEMW	INTR (Thru RST Circuit)
8085	RD	WR	INTR (Thru RST Circuit)
Z-80	RD	WR	INT (Thru RST Circuit, Mode 0)
SC/MP	NRDS	NWDS	SA (Thru Sense A)
6800	VMA•φ2•R/W	VMA•φ•R/W	IRQA or IRQB (Thru PIA)

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Dual-In-Line Package (N)
Order Number ADC0808CCN or ADC0809CCN
NS Package Number N28B



Molded Chip Carrier (V)
Order Number ADC0808CCV or ADC0809CCV
NS Package Number V28A

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