

Sudan University of Science & Technology

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Adaptive Gain Control for Parabolic Reflector
Antenna Using Real Time Embedded system

التحكم بكسب الهوائى ذو القطاع المكافئ باستخدام الانظمة المدمجة
بالزمن الحقيقى

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بِسْمِ اللَّهِ الرَّحْمَنِ الرَّحِيمِ

قَالُوا سُبْحَانَكَ عِلْمٌ لَنَا إِلَّا مَا عَلَّمْتَنَا إِنَّكَ أَنْتَ

الْعَلِيمُ الْحَكِيمُ

سورة البقرة- (٣٢)

Dedication

To my parents and family

ACKNOWLEDGEMENTS

In the name of Allah, the Most Gracious and the Most Merciful

All praises and glory be to Allah for blessing me with opportunities abound and showering upon me his mercy and guidance all through the life. I pray that He continues the same the rest of my life. And may his peace and blessings of Allah be upon Prophet Muhammad, a guidance and inspiration to our lives.

I would like to thank my supervisors, **Dr.** Abdelrasoul jabar kizar alzubaidi for his guidance and expertise throughout this thesis. There was always there when I needed him, and even with his tight schedule, he has always found time for me.

I am extremely grateful to him for his prompt replies and his numerous proofreads. I am special thanks to my colleagues and friends for their encouragements and various help that they provided throughout my study. I would like to give my special thanks to my parents and my wife for their support, patience and love. Without their encouragement, motivation and understanding it would have been impossible for me to complete this work.

ABSTRACT

The study aims to investigate the gain of parabolic reflector antenna control by using real time embedded system .In turn the control of parabolic reflector antenna leads to control of antenna radiation which is the main element to transmit and receive signal for wireless communication.

This study is about system design of control of parabolic reflector antenna gain which plays the main goal of using the parabolic reflector antenna for long distance communication systems (satellite, radar and microwave transmission lines). The parabolic antenna is characterized by high gain, here we use the helical antenna as feeder of parabolic reflector antenna to increase the gain and give the ideal polarization which is requested at satellite communication.

The methodology of this study is composed of the control of dish diameter using real time embedded system to increase and decrease the parabolic dish diameter size, which is the main parameter in terms of gain. The system controls the helical antenna (feeder) by controlling the gain by real time embedded system. The device and algorithm described is enough compact and simple to be suitable for all goals of wireless communication systems and it is very ideal for radar and telecom microwave transmission systems.

Practical and simulation result show the increase of gain according to the increase of parabolic dish diameter, and control the gain of helical antenna until obtaining the optimum value for gain.

المستخلص

تهدف الدراسة الى تحرى التحكم فى كسب الهوائى ذو القطاع المكافئ باستخدام الانظمة المدمجة بالزمن الحقيقى.

ان التحكم فى الهوائى ذو القطاع المكافئ يقود بدوره الى التحكم فى الاشعاع الصادر منه الذى يعتبرالعنصر الاساسى فى ارسال واستقبال اشارة الاتصالات الاسلكية.

هذه الدراسة عبارة عن تصميم نظام للتحكم فى كسب الهوائى ذو القطاع المكافئ الذى يمثل الهدف الرئيسى فى استخدام الهوائى ذو القطاع المكافئ فى الاتصالات ذات المسافات البعيدة مثل اتصالات الاقمار الصطناعية، انظمة الرادار و خطوط نقل الموجات الدقيقة. من اهم صفات الهوائى ذو القطاع المكافئ الكسب العالى، فى هذه الدراسة سنستخدم الهوائى الحلقى كمغذى للهوائى ذو القطاع المكافئ لزيادة الكسب واعطاء استقطاب مثالى مطلوب بالنسبة لاتصالات الاقمار الاصطناعية.

طريقة البحث تتألف من التحكم فى قطر طبق الهوائى ذو القطاع المكافئ باستخدام محرك الخطوة متحكما فيها بواسطة الدوائر المدمجة لزيادة ونقصان قطر طبق الهوائى ذو القطاع المكافئ الذى يعتبر المتغير الاساسى فى تغيير الكسب. النظام ايضا يتحكم فى الهوائى الحلقى المغذى.

المكونات والخوارزمية وصفت بشكل موثق وبسيط ليكون مناسباً لجميع اهداف الاتصالات الاسلكية ومثالى لانظمة الرادار ونظم خطوط نقل الموجات الدقيقة للاتصالات.

نتائج التجارب وبرامج المحاكاة تعرض وتوضح زيادة الكسب تبعا لزيادة قطر طبق الهوائى ذو القطاع المكافئ وكسب الهوائى الحلقى حتى تم التحصل على القيم المثلى لكسب المغذى.

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List of Symbols

C	capacitance [F]	Cd	drag coefficient	
D	dish diameter			
D	is the diameter. (The circumference divided by π			
C	Circumference			
c	light speed			
f	frequency used			
G	antenna gain,			
H	magnetic field strength [A/m]			
J	current density [A/m ²]			
Jm	magnetic current density [V/m ²]	k	wave number [1/m]	
n	unit normal vector-			
N	NO of turns of helical antenna			
P	power [W]			
P _{in}	input power [W]			
P _{rad}	radiated power [W]			
r	far field distance, observation distance, distance [m], normalized distance			
	r	field coordinate	r	source coordinate
R	resistance [Ω]			
S	turn spacing			
U	radiation intensity [W/unit solid angle]			
Z ₀	characteristic impedance [Ω]			
Z _L	load impedance [Ω]			
S	is the spacing from turn to turn.			

List of Abbreviations

ACSR	Analog Comparator Control and Status Register
ADC	Analog to Digital Converter
ADCH	High byte of ADC result
AC	alternating current
ADCL	Low byte of ADC result
ADCSRA	ADC Control and Status Register
ADCW	Analog to Digital Word
ADMUX	ADC Multiplexer Register
ALU	Arithmetic Logical Unit
ARFF	Analog Reference
AR	axial ratio
AVCC	Analog Collector Control Voltage
CPU	Control processing unit
DAC	Digital to Analog Converter
DC	direct current
DDR	Data Direction Register
DDRA	Data Direction Register Port A
DDRB	Data Direction Register Port B
DDRC	Data Direction Register Port C
DDRD	Data Direction Register Port D
EEPROM	Electronic Erasable Programmable Read-Only Memory
GND	Ground

ISP	In System Programming
IL	insertion loss
LCD	liquid crystal display
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SLR	side lobe ratio
SWR	standing wave ratio
TEM	transverse electromagnetic
TCCR1	Timer/Counter Control register
TCCR1A	Timer/Counter Control register Port A
TCCR1B	Timer/Counter Control register Port B
TWI	Two Wire Interface
VCC	Voltage Common Cathode
VSWR	voltage standing wave ratio
XTAL1	Crystal clock Input 1
XTAL2	Crystal clock Input 2

Chapter One

Introduction

1.1 Overview

The idea of using parabolic reflectors for radio antennas has taken from optics where is the power of a parabolic mirror to focus light into a beam has been known since long time ago the first parabolic antenna used for satellite communications was constructed in early sixties, to communicate with the satellite. The advent in the computer programs capable of calculating the radiation pattern of parabolic antennas has led to the development of sophisticated asymmetric, multi reflector and multi feed designs in recent years. The helical feed parabolic antenna meets many applications. There is a possibility to control the parabolic dish dimensions as well as the helical feed length. BY applying the two controls give a change of the antenna gain. Hence an automatic antenna gain control will be produced.

1.2 Background

As mention above the parabolic reflector antenna has been used widely in application for many projects of wireless communications especially for long distance satellite communication, radar and sensitive telecom fields. it is characterized by high gain which is the main points of transmitting and receiving signal .There are many problems on fields prevent to transmitting and receiving good signal in terms of weather problem raining, dust and humidity. Graphical topology of transmission area and earth plasma also is effect of

problems. By controlling of antenna parameters the weakness of signal will be compensated to avoid any disturbance.

1.3 Problem Statement

The main problem leads to search, investigate, analyze and build new system to control parabolic reflector antenna so as to have optimum solution to the weakness of received signal, according to weather problem effects on transmission quality .According to antenna transmission equation that received signal depends upon many parameters such as power, gain of antenna, frequency of signal and distance between antennas as well as transmission path .Weakness of received signal will leads to received signal loosing .Therefore a new system to compensate the weakness of signal should be build to avoid loosing of signal and to maintain transmission line between antennas from errors which are led to many transmission problems

1.4 Objectives

The objective of this study attempts to find out some solution to investigate system problem such as weakness reception of parabolic reflector antenna. There are many objectives of this study:

- Control of gain of parabolic reflector antenna by control of parabolic dish diameter (D) and control of helical (parabolic reflector antenna feeder) length
- Automated the control of parabolic gain using microcontroller and feedback received signal
- Get high gain of parabolic reflector antenna to find and sustain the signal transmit and receive between antennas with high performance and good quality
- keep all solution simple and easy to construct for early stage prototyping

1.5 Significance of the Study:

Parabolic reflector antenna has played a vital role in telecommunication industry and the antenna gain is carried out to insure good transmitting and receiving level.

In the various research conducted, it can be deduced that parabolic reflector antenna gain is not of job to complete, in fact it is critical in roll out implementation phase as well as operation and maintenance. Even with high gain of antenna, it is notice that the good receiving and

transmitting signal and it is avoid the weakness of path signal .there could be multiple reasons behind weakness of signal such as environmental condition and obstruction in the path tow station .

This research is deal with the rectification and find out solution of this problem by controlling the gain of parabolic reflector antenna gain which lead to sustainable of transmitting and receiving signal id the dedicated value and avoid the weakness of signal

The process that is involved in MW link alignment and gain enhancement demand very sophisticated staff and test equipment .in addition the high number of man hours that are required to perform alignment, replacement antenna, arranging and mobilization the equipment is also concern .if the received signal is beyond the acceptable rang than a huge losses that are incurred because active link which is carried the traffic is disrupted .according to study in METE group [in 2008].it was reported that the cost of down time in telecom industry is \$2million/hour.

Generally when the link is reported to be down, it takes 4 hours on average to reach and certify the problem in city and 6 hours on average to fix in distant places.

A solution which can reduce the downtime and ultimately reduce the financial and service losses is always desired and this has driven the research conducted on this study.

1.6 Methodology of the Study

The researcher will use two methods to conduct this study. Those methods are divided in to hardware system and software system.

The hardware system is based on using a microcontroller as a processor. Interface circuits are connected to the microcontroller. A matrix keypad is connected to the microcontroller for data entry .An LCD is connected to a port of the microcontroller to display data. Four stepper motors are connected to the interface circuit in order to control the four sectors of the parabolic reflector of the antenna. A stepper motors is connected to the interface circuit in order to control the helix feed of the antenna.

The software design is performed by programming the main controller circuit (atmega32) which is connected to an interface circuit designed to drive the stepper motors .The software package used here is BASCOM. BASCOM is an Integrated Development Environment (IDE) that supports the Atmel's AVR microcontrollers.

1.7 Thesis Layout

The research contains five chapters as the following:

Chapter two present literatures review and give the overview and background about antenna, microcontroller and stepper motor. The following topics will be discussed also the previous studies of the felid. Chapter three discusses the system design. Which is split for two

section, firstly hardware design, describes the circuit composed and operation with help of schematic diagrams .In addition to detailed explanations for circuit's components. Second section about software design program used to control of system.

Chapter four includes results and discussion.

Chapter five covers the conclusion and future recommendations

Then list of references will be sited at the end of the thesis, plus the appendix

Chapter Two
Literature review and
Background

2.1 Preface

This research is concerned with designing system to control parabolic reflector antenna gain which consist of two part, parabolic dish control and parabolic reflector antenna feeder (helical antenna) control

The main components of this research system design are parabolic reflector antenna, helical antenna; stepper motor and microcontroller. Short introduction to the component are specific within scope of this chapter

2.2 Antenna

Many text books on antenna and practice have been written. However ,a short introduction to those concepts that are specific importance within scope of this work are presented in this chapter .A more detailed treatment of topics related to antenna design can be found, e.g., in references [1]

2.2.1 Antenna theory

An antenna is metallic device for radiating or receive radio wave .Flowing current in an antenna structure generate an electromagnetic field .Apart of this field remaining near the antenna and the reset is radiated in to the surrounding space .On the other hand ,electromagnetic field received at the antenna generate current in it. In addition to receiving or transmitting energy, an antenna in an advanced wireless [2]

System is usually required to optimize or to send the radiation energy in some direction and suppress it in to other .Thus the antenna must also serve as directional devise in addition to radiation deiced. It must then take various forms to meet the

particular need at hand, and it may be a piece of conducting wire, an aperture, a patch, an assembly of elements (array), a reflector, a lens, and so forth.

2.2.2 Antenna radiation

The radiated field of a general current density $J(\mathbf{r})$ satisfies Maxwell's equations and can be calculated, for example, from a wave equation using the concept of vector potential. If all boundary conditions are also known, the radiated field of the antenna can be calculated. Unfortunately, determining the currents of a real antenna with sufficient accuracy is usually too difficult or even impossible in practice. Even if this could be done, the resulting equations would still be very difficult to solve. However, they can be approximated by considerably simpler equations if the distance to the antenna is large and if the complicated current densities can be replaced with simpler equivalent sources.

In the far field, radiation properties of an antenna do not depend considerably on observation distance, and the radiated wave front is essentially spherical. A generally used criterion is that the phase difference of the radiated fields from different parts of the antenna must be smaller than $\pi/8$ in the far field. According to this condition, the far field begins at a distance of

$$r = \frac{2d^2}{\lambda} \quad (2.1)$$

Where d is the largest dimension of the antenna and λ is the wavelength. Equation (2.1) holds if $d > \lambda$, but it usually works well also for smaller antennas.

Radiated electric (E) and magnetic (H) fields of a time-harmonic current source are related in the far field by

$$\mathbf{E}(\mathbf{r}) \approx -\eta \mathbf{u}_r \times \mathbf{H}(\mathbf{r}), \quad (2.2)$$

Where r is the field coordinate, \mathbf{u}_r is the radial unit vector, $\eta = \sqrt{\mu/\epsilon}$ is the wave impedance (about 377 Ω in air and vacuum), μ is the permeability, and ϵ is the permittivity of the surrounding medium. In other words, the radiated wave is transverse electromagnetic (TEM). Fields can be solved using Equation (2.2) in accordance with

$$\mathbf{H}(\mathbf{r}) \approx -jk \frac{e^{-jkr}}{4\pi r} \mathbf{u}_r \times \int_V e^{-jk\mathbf{u}_r \cdot \mathbf{r}'} \mathbf{J}(\mathbf{r}') dV', \quad (2.3)$$

where \mathbf{r}' is the source coordinate, k is the wave number, and r is the observation distance.

2.2.3 Antenna parameters

To describe the properties of antennas, numerous parameters are needed. Any antenna can be considered as a radiating (or intercepting) structure but also as a circuit element. Important parameters from a radiating viewpoint include (at least) radiation pattern, directivity, beam width, polarization, and effective area. As a circuit element, an antenna will have, for example, some input impedance and efficiency. In addition, few other parameters such as manufacturability, size, weight, and cost should also be kept in mind when designing antennas. The most important parameters concerning the work of this thesis are shortly discussed next.

Radiation pattern, or antenna pattern, describes the radiation properties of an antenna as a function of space coordinates. It can be a

mathematical function or a graphical representation of, e.g., radiation intensity, field strength, field phase, or polarization. Despite its broad definition, the antenna pattern usually describes the spatial distribution of radiated energy in terms of field strength or radiated power. Especially with linearly polarized antennas, plane cuts in principal planes are often used: the E-plane contains the direction of maximum radiation and the electric field vector; the H-plane contains the direction of maximum radiation and the magnetic field vector. As an example, a plane cut of a radiation pattern in Cartesian coordinates is presented in Figure (2.1).

Regions in the antenna pattern bounded by relatively weak radiation are referred to as lobes. The one containing the direction of maximum radiation is called the main lobe (or the main beam), all other lobes are side lobes. A back lobe is the side lobe pointing approximately in the opposite direction than the main lobe. Relative magnitudes of the main lobe and the side lobes can be evaluated by using a side lobe ratio (SLR), which is the ratio of the main lobe amplitude to the highest side lobe amplitude. The width of a lobe is described using beam width, which is the angular region between the directions for which the amplitude is dropped by a certain amount from its maximum value within the lobe. Usually a half power beam width θ_{3dB} is used, but sometimes other criteria are chosen instead, for example 1 dB drop or the angle between first pattern nulls.

An antenna is said to be directive if it radiates more effectively to some directions than to others. According to this definition, all realizable antennas are directive. The directivity of an antenna (D) is defined as

the ratio of its radiation intensity in a given direction to the average radiation intensity. The most common reference for directivity is an imaginary [2]

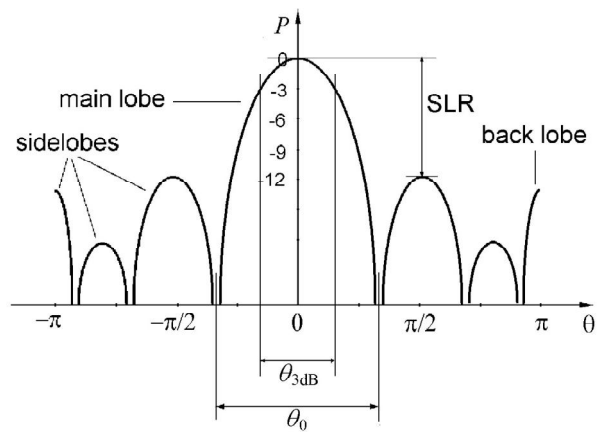


Figure (2.1) a plane cut of a three-dimensional radiation pattern: lobes, Side lobe ratio (SLR) and beam widths

In many times is not sufficient to consider only directivity since all the power feeded in the antenna is not radiated, but some of it is dissipated due to dielectric and conduction losses. Taking account of these losses, antenna gain can be defined as:

$$G(\mathbf{u}_r) = \frac{4\pi U(\mathbf{u}_r)}{P_{in}} = e_{cd} \frac{4\pi U(\mathbf{u}_r)}{P_{rad}} = e_{cd} D(\mathbf{u}_r) \quad (2.4)$$

where U is the radiation intensity, P_{in} is the input power, P_{ad} is the radiated power, and e_{cd} is the radiation efficiency. One should remember that this is not the overall efficiency of a real world antenna system because it does not include impedance mismatch or polarization mismatch losses.

The polarization of an antenna in a given direction is defined as the polarization of the wave it radiates. The polarization of the radiated wave describes the behavior of its electric field vector over time, observed along the direction of propagation. In a general case the tip of the E-vector draws an ellipse in a plane perpendicular to the direction of propagation, and the polarization is said to be elliptical. Important special cases of the elliptical polarization are linear and circular polarizations. If the E-vector rotates clockwise, the polarization is right-handed, otherwise left-handed. The amount of polarization ellipticity is measured with an axial ratio (AR), which is the ratio of the major and minor axes of the polarization ellipse. In many cases it is convenient to resolve the polarization characteristics into two components: the desired one is called co-polarized and the other one cross polarized.[3]

In the reception case, antenna polarization is defined as the polarization of the incoming wave giving maximum received power. If the polarization of a receiving antenna differs from the polarization of the incoming wave, polarizations are mismatched and additional loss is introduced. Polarization mismatch loss between co- and cross polarization is infinite in theory. However, in practice both polarization components are always present, and for linearly polarized antennas cross polarization levels are typically in the order of about -20 dB to -40 db.

Circuit properties of antennas are usually of interest because the impedance levels of the transmitter and the antenna have to be matched to ensure good power transmission, and in high power applications, to avoid equipment damage. Usually scattering parameters are used to describe the circuit properties of the antenna and its feed network. An antenna itself is a one port device, and reflected power in its feed is often expressed using return loss

$$RL = 20\log|S_{11}|. \quad (2.5)$$

In addition, another popular way to express the level of mismatch is to use voltage standing wave ratio

$$VSWR = \frac{1 + |S_{11}|}{1 - |S_{11}|}. \quad (2.6)$$

Losses in the feed network are described in a convenient way by using insertion loss, which is defined as:

$$IL = 20\log|S_{21}|. \quad (2.7)$$

In many cases it is important to know the bandwidth of the antenna, which is defined as the frequency region within which some of the antenna properties remain within some predefined and reasonable limits. Selection of that property and its limits depend on the application. Usually the limiting

property is impedance matching, but it can as well be, for example, gain or polarization.[2]

2.1.3 Aperture distributions

Radiation from aperture antennas (e.g., horns, lenses and reflectors) can be computed using an equivalence theorem. It states that the electromagnetic field in a source free region can be exactly computed from the distribution of electric and magnetic currents over the surface that encloses the sources. E- and H-fields at the aperture are used to compute a current density $\mathbf{J} = \mathbf{n} \times \mathbf{H}$ and an (imaginary) magnetic current density $\mathbf{J}_m = \mathbf{n} \times \mathbf{E}$ (\mathbf{n} is the unit normal vector of the surface). Generally speaking, this method may be intractable but on the other hand, is valid in all field regions.

If it is sufficient to consider radiation only in the far field, the task is considerably eased by assuming that electric and magnetic fields at the aperture are related as in a free space TEM-wave (equation (2.2)). In that case only an aperture distribution, i.e., the electric field strength at the aperture is needed. The far field pattern of the radiating aperture is the Fourier-transform of the aperture distribution if following conditions are met: (a) the aperture is finite, (b) observation distance is much greater than the aperture size, and (c) the observation distance is much greater than the wavelength [1]. Solving this two-dimensional transform for arbitrarily shaped aperture requires, in general, numerical integration techniques. However, three important special cases are considerably easier to calculate, namely linear, rectangular, and circular aperture distributions.

One-dimensional aperture distributions, the simplest of all, are called line sources. If the amplitude is constant, the distribution is said to be uniform. One may think of a signal in time and frequency domains to aid in visualizing a line source. In fact, a uniform linear distribution corresponds

to a time domain square pulse, which has a since-function ($\sin(x)/x$) shaped frequency response through Fourier transform. Mathematically the relation between source coordinates and radiation pattern angles is similar for a line source, and its far field pattern

$$F(\theta) = \frac{\sin(\pi u)}{\pi u}, \quad u = \frac{L}{\lambda} \sin(\theta) \quad (2.8)$$

Where θ is the angle of radiation measured from direction perpendicular to the source dimension and L is the length of the source. Since the distribution has only one dimension, its pattern is rotationally symmetric. As an example, a pattern of 70 wavelengths long uniform line source in the vicinity of the main beam is illustrated in Figure 2.2.

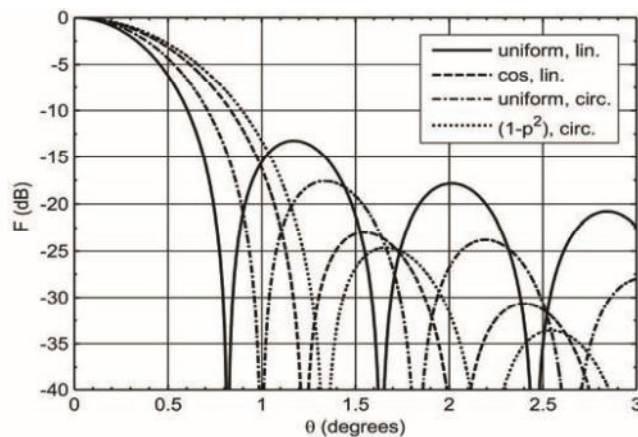


Figure (2.2) Examples of far field patterns of different aperture distributions. Line source length / aperture diameter is 70 wavelengths. Many kinds of linear distributions have been invented to aid analysis and design.

2.3 Reflector antennas

Sufficiently high gain values for applications such as radar can only be achieved either using phased arrays or reflector antennas. For a simple pencil beam (i.e., main beam narrow in all planes) pattern requirement, phased arrays are usually far too complex and expensive, thus making a reflector more attractive. A typical high gain reflector antenna system consists, in principle, of a relatively large reflector and a low gain primary feed radiator. More complicated systems may include several reflectors and feed antennas. In addition to these, feed lines, mounting structures, and possibly mechanical rotating, steering, and random (a housing that protects the antenna from weather) structures are needed. Those aspects of single reflector antenna design that are the most relevant to this thesis are discussed in the following. [2]

2.3.1 Parabolic reflector

A parabolic dish is by far the most commonly used reflector for the micro- and millimeter wave regions. This is due to the fact that a parabolic is the only three-dimensional shape that focuses parallel rays to a single focal point. Other geometries are occasionally used, for example, spherical reflectors in applications requiring wide angle scanning capability. In dual reflector systems the main parabolic is illuminated via a sub reflector, which is sometimes elliptical (Gregorian system) but usually hyperbolic (Cass grain system). The main reason for using an additional sub reflector is to make the overall antenna more compact but it also gives more degrees of freedom in design. Very sophisticated antenna systems may have complex, numerically designed surfaces, e.g., to compensate for various kinds of phase errors in the system or to shape the main beam. [2]

Parabolic reflector geometry is illustrated in Figure (2.3). A parabolic is formed by rotating a piece of a parabola around the z-axis. Curvature of a parabolic reflector is normally expressed using its f/d-ratio which is the ratio of the focal length f to the diameter d .

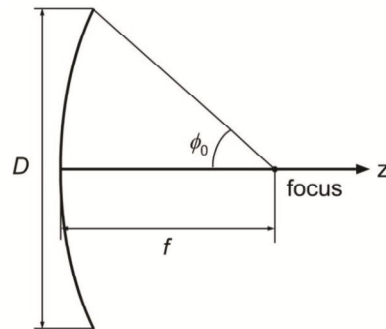


Figure (2.3) parabolic reflector geometry:

D is the diameter of the reflector.

Typically f/d -ratios are in the range of 0.2 - 1 [1]. Smaller f/d -ratios result in shorter antennas, but on the other hand also in more degraded performance due to various aberrations. In radio link and radio astronomy applications reflectors typically have a circular contour (thus often called a "dish"). However, in radar applications circular rims are not encountered as often as elliptical ones ("orange peel"), which are common. The reason for this is the need to generate a fan-shaped beam, which is achieved by narrowing the aperture in one principal plane.

All reflecting systems suffer from various kinds of aberrations. They are originated either from the geometry or the imperfections in the feed, reflector, or both. Aberrations cause the phase front to deviate from the ideal uniform. If the imperfections are not taken into account, the phase front across the aperture can be expressed in the form of an infinite series:

$$\Phi(r) = 1 + \beta_1 r + \beta_2 r^2 + \beta_3 r^3 + \beta_4 r^4 \dots, \quad (2.9)$$

where r is the normalized aperture dimension and β 's are the phase errors at the aperture edge. The most important in designing high gain reflectors are the first four, commonly called linear, focus, coma, and spherical aberrations. [1]

The first order linear aberration is simply a linear phase shift over the aperture. It only changes the direction of the phase front, turning the pattern in angular space. Linear phase shift is generated by laterally displacing the feed from the focal point. The second order focus aberration is generated if the feed is displaced from the focal point in axial direction. This does not affect beam pointing but decreases directivity, broadens the main beam, and blends the side lobes into the main beam. Displacing the feed laterally in the focal plane causes also problems. Because simple reflectors do not satisfy Abbe's sine condition (e.g., dual reflector Schwarzschild system would be needed [10]), the third order coma aberration is generated. The amount of the coma error depends on the displacement and the f/d ratio of the system. A main beam tilt and an unsymmetrical pattern are the consequences of coma. Side lobes on bore sight are higher than on the other side, the highest side lobe (next to the main beam) often called a coma lobe. In addition, lateral displacement of the feed also introduces astigmatism, which causes the focal lengths for the two principal planes to differ. Fourth order aberration is called spherical, and it has similar effects than the second order focus error. In practice, a reflector antenna system performance will always be degraded due to aberrations because the phase center of the feed antenna is not a dimensionless point and also because it moves with the operating frequency.

Depolarization and surface errors deteriorate reflector performance and may also be considered as aberrations. Oblique reflection is the cause of

depolarization, i.e., part of the radiated energy is converted to the cross-polarized component. The level of depolarization is increased with decreasing f/d -ratio due to larger surface curvature. Surface errors can be regular or random. Regular surface errors affect mainly the phase of the aperture distribution. In practice, it is sufficient to consider four types of regular errors: linear, quadratic, cubic, and periodic. First three have similar effects than linear, focus and coma errors, treated in the previous paragraph. Periodic errors typically produce large grating lobes (multiples of the main beam), just like in an array antenna. Random surface errors, e.g. due to surface roughness, increase side lobe envelope and decrease directivity [3]

2.3.1.1 Parabolic reflector antenna types

Parabolic antennas are distinguished by their shapes:

- Parabolic or dish

The reflector is shaped like a parabolic. This is the most common type. It radiates a narrow pencil-shaped beam along the axis of the dish.

- Shrouded dish

Sometimes a cylindrical metal shield is attached to the rim of the dish. The shroud shields the antenna from radiation from angles outside the main beam axis, reducing the side lobes. It is sometimes used to prevent interference in terrestrial microwave links, where several antennas using the same frequency are located close together. The shroud is coated inside with microwave absorbent material. Shrouds can reduce back lobe radiation by 10 db. [2]

The reflector is curved in only one direction and flat in the other. The radio waves come to a focus not at a point but along a line. The feed is sometimes a dipole antenna located along the focal line. Cylindrical parabolic antennas

radiate a fan-shaped beam, narrow in the curved dimension, and wide in the incurved dimension. The curved ends of the reflector are sometimes capped by flat plates, to prevent radiation out the ends, and this is called a pillbox antenna.

Modern parabolic antennas can be designed to produce a beam or beams of a particular shape, rather than just the narrow "pencil" or "fan" beams of the simple dish and cylindrical antennas above. Two techniques are used, often in combination, to control the shape of the beam Shaped reflectors - With a single feed antenna, the only option is to alter the shape of the reflector(s). The parabolic reflector can be given a noncircular shape, and/or different curvatures in the horizontal and vertical directions, to alter the shape of the beam. This is often used in radar antennas.

- "Orange peel" antenna

Used in search radars, this is a long narrow antenna shaped like the letter "C". It radiates a narrow vertical fan shaped beam.

- Arrays of feeds

In order to produce an arbitrary shaped beam, instead of one feed horn an array of feed horns clustered around the focal point can be used. Array-fed antennas are often used on communication satellites, particularly direct broadcast satellites, to create a downlink radiation pattern to cover a particular continent or coverage area. They are often used with secondary reflector antennas such as the Cass grain.

Parabolic antennas are also classified by the type of feed, that is, how the radio waves are supplied to the antenna:

- Axial or front feed – This is the most common type of feed, with the feed antenna located in front of the dish at the focus, on the beam axis. A

disadvantage of this type is that the feed and its supports block some of the beam, which limits the aperture efficiency to only 55 - 60%.^[2]

-Off-axis or offset feed - The reflector is an asymmetrical segment of a parabolic, so the focus, and the feed antenna, is located to one side of the dish. The purpose of this design is to move the feed structure out of the beam path, so it doesn't block the beam. It is widely used in home satellite television dishes, which are small enough that the feed structure would otherwise block a significant percentage of the signal. Offset feed is also used in multiple reflector designs such as the Cassegrain and Gregorian, below.

-Cass grain - In a Cassegrain antenna the feed is located on or behind the dish, and radiates forward, illuminating a convex hyperbolic secondary reflector at the focus of the dish. The radio waves from the feed reflect back off the secondary reflector to the dish, which forms the outgoing beam. An advantage of this configuration is that the feed, with its waveguides and "front end" electronics does not have to be suspended in front of the dish, so it is used for antennas with complicated or bulky feeds, such as large satellite communication antennas and radio telescopes. Aperture efficiency is on the order of 65 - 70% [2]

-Gregorian - Similar to the Cassegrain design except that the secondary reflector is concave, (ellipsoidal) in shape. Aperture efficiency over 70% can be achieved.

2.3.1.2 Parabolic reflector antenna Parameters

1- Gain:

The directive qualities of an antenna are measured by a dimensionless parameter called its gain, which is the ratio of the power received by the antenna from a source along its beam axis to the power received by a hypothetical isotropic antenna. The gain of a parabolic antenna is:

$$G = \frac{4\pi A}{\lambda^2} e_A = \frac{\pi^2 d^2}{\lambda^2} e_A \quad 2.11$$

Where:

A is the area of the antenna aperture, that is, the mouth of the parabolic reflector

d is the diameter of the parabolic reflector

λ Is the wavelength of the radio waves?

e_A is a dimensionless parameter between 0 and 1 called the aperture efficiency. The aperture efficiency of typical parabolic antennas is 0.55 to 0.70.

It can be seen that, as with any aperture antenna, the larger the aperture is, compared to the wavelength, the higher the gain. The gain increases with the square of the ratio of aperture width to wavelength, so large parabolic antennas, such as those used for spacecraft communication and radio telescopes, can have extremely high gain. Applying the above formula to the 25-meter-diameter antennas often used in radio telescope arrays and satellite

ground antennas at a wavelength of 21 cm (1.42 GHz, a common radio astronomy frequency), yields an approximate maximum gain of 140,000 times or about 50 dBi (decibels above the isotropic level).

Feed spillover - Some of the radiation from the feed antenna falls outside the edge of the dish and so doesn't contribute to the main beam.

Feed illumination taper - The maximum gain for any aperture antenna is only achieved when the intensity of the radiated beam is constant across the entire aperture area. However the radiation pattern from the feed antenna usually tapers off toward the outer part of the dish, so the outer parts of the dish are "illuminated" with a lower intensity of radiation. Even if the feed provided constant illumination across the angle subtended by the dish, the outer parts of the dish are farther away from the feed antenna than the inner parts, so the intensity would drop off with distance from the center. So the intensity of the beam radiated by a parabolic antenna is maximum at the center of the dish and falls off with distance from the axis, reducing the efficiency.

Aperture blockage - In front-fed parabolic dishes where the feed antenna is located in front of the dish in the beam path (and in Cassegrain and Gregorian designs as well), the feed structure and its supports block some of the beam. In small dishes such as home satellite dishes, where the size of the feed structure is comparable with the size of the dish, this can seriously reduce the antenna gain. To prevent this problem these types of antennas often use an offset feed, where the feed antenna is located to one side, outside the beam area. The aperture efficiency for these types of antennas can reach 0.7 to 0.8.

The gain of antenna is affect directly for the power received by antennae according to below equation

$$P_r = \frac{P_t G_t G_r \lambda^2}{4\pi r^2} \quad 2.12$$

Where P_r is signal receive

P_t is transmit signal

G_r the gain of receive antenna

G_t the gain of transmit antenna

λ is wave length

r is distance between transmitter and receiver

2-Beam width:

The angular width of the beam radiated by high-gain antennas is measured by the half-power beam width (HPBW), which is the angular separation between the points on the antenna radiation pattern at which the power drops

$$\theta = k\lambda/d \quad 2.13$$

to one-half (-3 dB) its maximum value. For parabolic antennas, the HPBW θ is given by:

Where k is a factor which varies slightly depending on the shape of the reflector and the feed illumination pattern. For a "typical" parabolic antenna $k = 70$ when θ is in degrees.

For a typical 2 meter satellite dish operating on C band (4 GHz), like the one shown at right, this formula gives a beam width of about 2.6°. For the Arecibo antenna at 2.4 GHz the beam width is 0.028°. It can be seen that parabolic antennas can produce very narrow beams, and aiming them can be a problem. Some parabolic dishes are equipped with a bore sight so they can be aimed accurately at the other antenna.

It can be seen there is an inverse relation between gain and beam width. By combining the beam width equation with the gain equation, the relation is:___

$$G = \left(\frac{\pi k}{\theta} \right)^2 \epsilon_A \quad 2.14$$

2.3.1.3 Practical Dish Antennas

When we first described a parabolic dish antenna, we put a point source at the focus, so that energy would radiate uniformly in all directions both in magnitude and phase. The problem is that the energy that is not radiated toward the reflector will be wasted. What we really want is feed antennas that only radiates toward the reflector, and has a phase pattern that appears to radiate from a single point have a radiation patterns that drop off gradually at the edges, so the feed antenna is a compromise between acceptably low spillover and adequate illumination. For most front feed horns, optimum illumination is achieved when the power radiated by the feed horn is 10 dB less at the dish edge than its maximum value at the center of the dish. [2]

2.3.1.4 Parabolic reflector antenna feeder

The key to good parabolic dish antenna performance is the feed antenna, the source of radiated energy for the antenna system. There is a bewildering number of choices out there, and an equal number of opinions about which is best.

An optimum feed antenna for a parabolic dish reflector would have a radiation pattern which completely illuminates the reflector in both E- and H- planes with minimal spillover, as shown in Figure (2.4). A good feed also has the same phase center in both planes. A feed antenna must have a broad radiation pattern to illuminate a dish, much broader than the pattern of an antenna with reasonable gain. While the HDL_ANT program will do the calculations, it may be easier to understand the relationships visually. Figure 4-8 illustrates the desired illumination patterns for various f/D reflectors, and Figure 6.0-2 is a graph of illumination angle vs. f/D . Note that the relationship is not linear: the illumination angle for an $f/D = 0.6$ is not half the angle for an $f/D = 0.3$. [3]

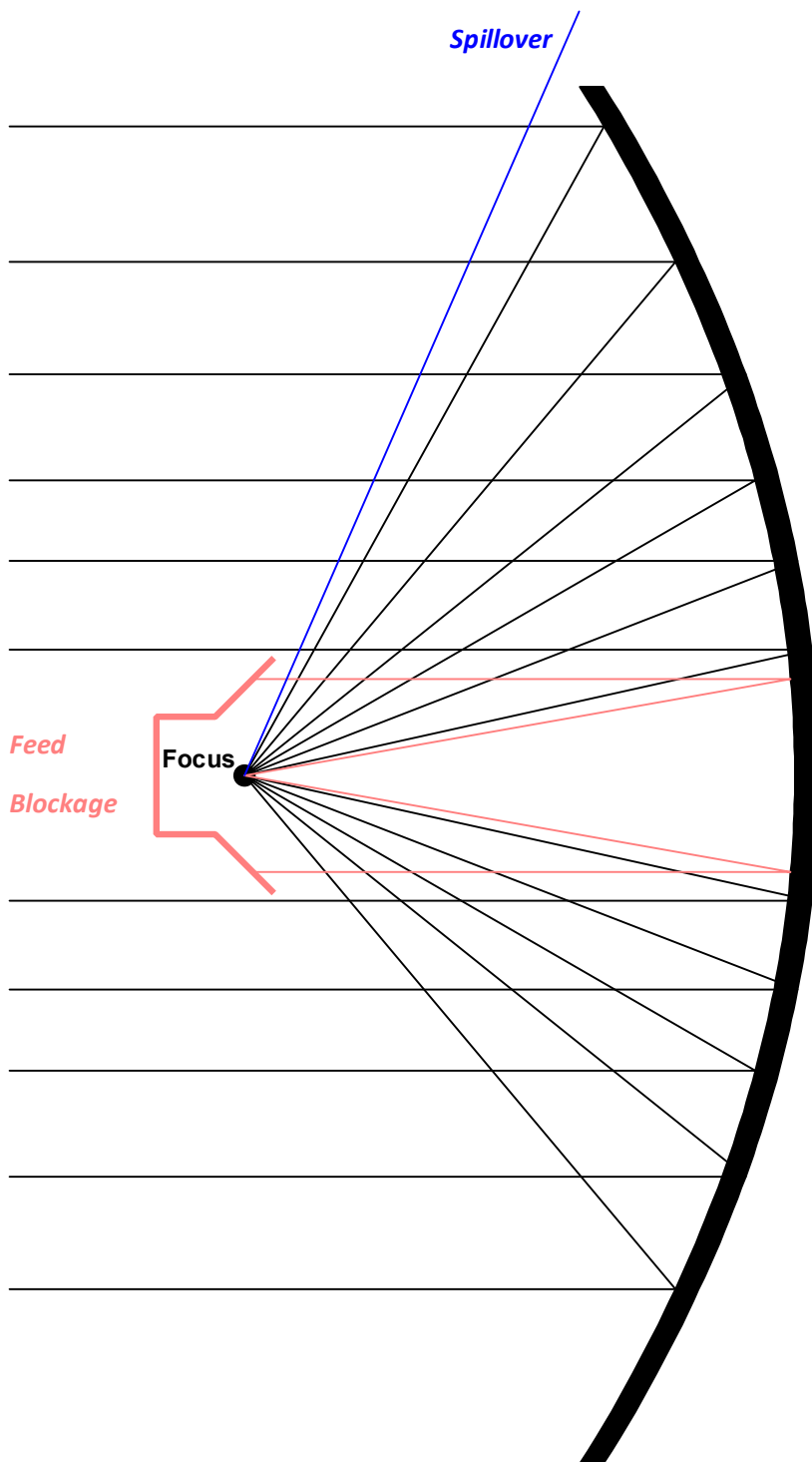


Figure (2.4) Geometry of parabolic dish antenna

2.4 Helical antennas

Helical antennas have long been popular in applications from VHF to Microwaves requiring circular polarization, since they have the unique Property of naturally providing circularly polarized radiation. One area that takes advantage of this property is satellite communications. Where more gain is required than can be provided by a helical antenna alone, a helical antenna can also be used as a feed for a parabolic dish for higher gains. As we shall see, the helical antenna can be an excellent feed for a dish, with the advantage of circular polarization. One limitation is that the usefulness of the circular polarization is limited since it cannot be easily reversed to the other sense, left-handed to right-handed or vice-versa.[7]

The helical antenna, first introduced by Kraus (1946), has been subject of extensive investigations during the past five decades. Many modifications to the basic helix geometry have been proposed with the aim of improving the gain, bandwidth, axial ratio, and VSWR. More recently, the possibility of size reduction, while maintaining the radiation characteristics, has been explored. In this paper, an improved performance antenna with a helical geometry is introduced. [6]

A helical antenna is an antenna consisting of a conducting wire wound in the form of a helix. In most cases, helical antennas are mounted over a ground plane. Helical antennas can operate in one of two principal modes: normal (broadside) mode or axial (or end fire) mode. The antenna then falls under the class of waveguide antennas, and produces true circular polarization. These antennas are best suited for space craft tracking and space

communication, where the orientation of the sender and receiver can be easily controlled.[6]

2.4.1 Helical antenna structure

This antenna, referred to as Helical Antenna is made of a primary helix wound on a cylinder of larger diameter. An important advantage of this antenna is that it can be conveniently constructed.



Figure (2.5) Structure of helical antenna

The helical antenna can be fully described by five parameters. The influence of these parameters on radiation properties are examined in order to find their optimum values.

2.4.2 Helical Optimum parameters

The effects of the helix parameters on radiation characteristics such as gain, input impedance, axial ratio, and bandwidth have been studied extensively.

A brief discussion of optimum parameters is presented below shows the effect of circumference on gain. The influence of pitch angle on gain at different frequencies. Clearly, a pitch angle of 12.5° provides the maximum gain. Kraus has developed empirical formulae for gain, input impedance, axial ratio, and half power beam width [6]

Kraus defines the pitch angle α as:

$$\alpha = \tan^{-1} \frac{s}{\pi D} \quad \dots\dots\dots (2.15)$$

Where;

S is the spacing from turn to turn.

D is the diameter. (The circumference divided by π)

The empirical gain formula is given

$$G = \frac{6.2C^2NS}{\lambda^3} = \frac{6.2C^2NSf^3}{c^3} \quad \dots\dots\dots (2.16)$$

- 1-G is helical antenna gain
- 2- C is Circumference
- 3- N is NO of turns of helical antenna
- 4- S is turn spacing
- 5-f is frequency used
- 6-c is light speed

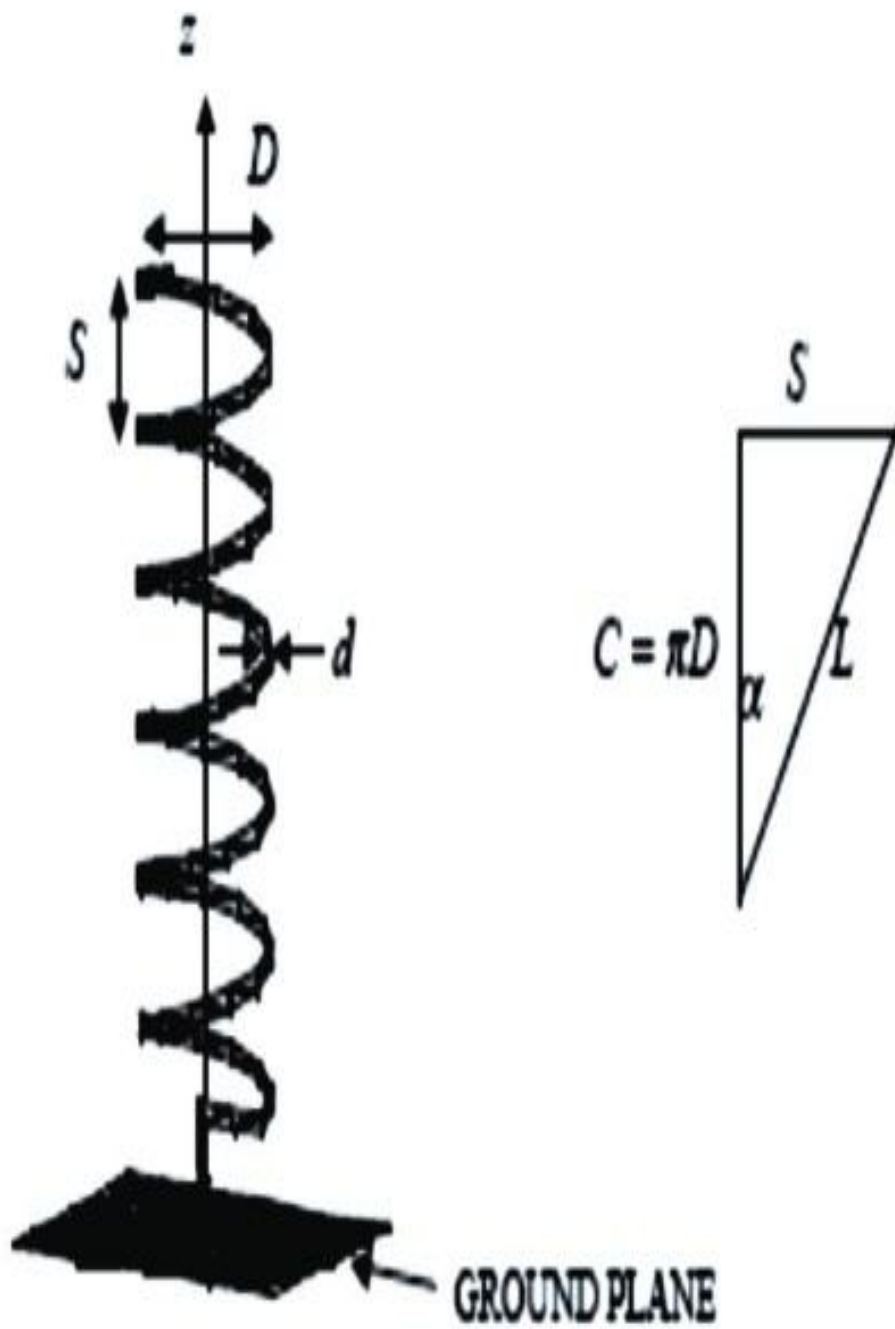


Figure (2.6) Cyclical Helix

2.5 Stepper motor

A stepper motor is an electromechanical device which converts electrical pulses into discrete mechanical movements. The shaft or spindle of a stepper motor rotates in discrete step increments when electrical command pulses are applied to it in the proper sequence. The motors rotation has several direct relationships to these applied input pulses. The sequence of the applied pulses is directly related to the direction of motor shafts rotation. The speed of the motor shafts rotation is directly related to the frequency of the input pulses and the length of rotation is directly related to the number of input pulses applied basics [8]

2.5.1 Stepper Motor Advantages and Disadvantages

Advantages

1. The rotation angle of the motor is proportional to the input pulse.
2. The motor has full torque at standstill (if the windings are energized)
3. Precise positioning and repeatability of movement since good stepper motors have an accuracy of 3 – 5% of a step and this error is non-cumulative from one step to the next.
4. Excellent response to starting/stopping/reversing.
5. Very reliable since there are no contact brushes in the motor. Therefore the life of the motor is simply dependent on the life of the bearing.
6. The motors response to digital input pulses provides open-loop control, making the motor simpler and less costly to control.
7. It is possible to achieve very low speed synchronous rotation with a load that is directly coupled to the shaft.
8. A wide range of rotational speeds can be realized as the speed is proportional to the frequency of the input pulses.

Disadvantages

1. Resonances can occur if not properly controlled.
- 2-Not easy to operate at extremely high speeds

2.5.2 Stepper Motor Types

There are three basic stepper motor types. They are:

- Variable-reluctance
- Permanent-magnet
- Hybrid

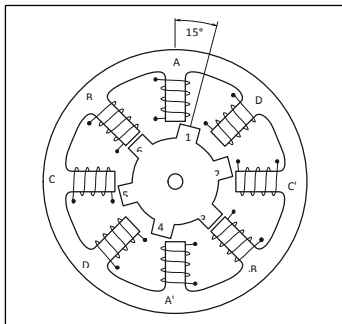


Figure (2.7) Principle of a disc stepper motor

Variable-reluctance (VR)

This type of stepper motor has been around for a long time. It is probably the easiest to understand from a structural point of view. Figure 1 shows a cross section of a typical V.R. stepper motor. This type of motor consists of a soft iron multi-toothed rotor and a wound stator. When the stator windings are energized with DC current the poles become magnetized. Rotation occurs when the rotor teeth are attracted to the energized stator poles.[9]

Permanent Magnet (PM)

Often referred to as a “tin can” or “can stock” motor the permanent magnet step motor is a low cost and low resolution type motor with typical step angles of 7.5° to 15° . (48 – 24 steps/revolution) PM motors as the name implies have permanent magnets added to the motor structure. The rotor no longer has teeth as with the VR motor. Instead the rotor is magnetized with alternating north and south poles situated in a straight line parallel to the rotor shaft. These magnetized rotor poles provide an increased magnetic flux intensity and because of this the PM motor exhibits improved torque characteristics when compared with the VR type.

Hybrid (HB)

The hybrid stepper motor is more expensive than the PM stepper motor but provides better performance with respect to step resolution, torque and speed. Typical step angles for the HB stepper motor range from 3.6° to 0.9° (100 – 400 steps per revolution). The hybrid stepper motor combines the best features of both the PM and VR type stepper motors. The rotor is multi-toothed like the VR motor and contains an axially magnetized concentric magnet around its shaft. The teeth on the rotor provide an even better path which helps guide the magnetic flux to preferred locations in the air gap. This further increases the detent, holding and dynamic torque characteristics of the motor when compared with both the VR and PM types.

The two most commonly used types of stepper motors are the permanent magnet and the hybrid types. If a designer is not sure which type will best fit his applications requirements he should first evaluate the PM type as it is normally several times less expensive. If not then the hybrid motor may be the right choice. [10]

There also exist some special stepper motor designs. One is the disc magnet motor. Here the rotor is designed as a disc with rare earth magnets, See fig. 4. This motor type has some advantages such as very low inertia and optimized magnetic flow path with no coupling between the two stator windings. These qualities are essential in some applications.

Size and Power

In addition to being classified by their step angle stepper motors are also classified according to frame sizes which correspond to the diameter of the body of the motor. For instance a size 11 stepper motor has a body diameter of approximately 1.1 inches. Likewise a size 23 stepper motor has a body diameter of 2.3 inches (58 mm), etc. The body length may however, vary from motor to motor within the same frame size classification. As a general rule the available torque output from a motor of a particular frame size will increase with increased body length.

Power levels for IC-driven stepper motors typically range from below a watt for very small motors up to 10 – 20 watts for larger motors. The maximum power dissipation level or thermal limits of the motor are seldom clearly stated in the motor manufacturer's data. To determine this we must apply the relationship $P = V \cdot I$. For example, a size 23 step motor may be rated at 6V and 1A per phase. Therefore, with two phases energized the motor has rated power dissipation of 12 watts. It is normal practice to rate a stepper motor at the power dissipation level where the motor case rises 65°C above the ambient in still air. Therefore, if the motor can be mounted to heat sink it is often possible to increase the allowable power dissipation level. This is important as the motor is designed to be and should be used at its maximum power dissipation, to be efficient from a size/output power/cost point of view [9]

2.5.3 Stepper motor application

A stepper motor can be a good choice whenever controlled movement is required. They can be used to advantage in applications where you need to control rotation angle, speed, position and synchronism. Because of the inherent advantages listed previously, stepper motors have found their place in many different applications. Some of these include printers, plotters, scanners, high end office equipment, hard disk drives, fax machines and many more. [8]

2.5.4 Stepper motor torque generation

The torque produced by a stepper motor depends on several factors.

- The step rate
- The drive current in the windings
- The drive design or type

In a stepper motor a torque is developed when the magnetic fluxes of the rotor and stator are displaced from each other. The stator is made up of a high permeability magnetic material. The presence of this high permeability material causes the magnetic flux to be confined for the most part to the paths defined by the stator structure in the same fashion that currents are confined to the conductors of an electronic circuit. This serves to concentrate the flux at the stator poles. The torque output produced by the motor is proportional to the intensity of the magnetic flux generated when the winding is energized.

2.5.5 Stepper motor Phases, Poles and Stepping Angles

Usually stepper motors have two phases, but three- and five-phase motors also exist. A bipolar motor with two phases has one winding/phase and a unipolar motor has one winding, with a center tap

per phase. Sometimes the unipolar stepper motor is referred to as a “four-phase motor”, even though it only has two phases.

Motors that have two separate windings per phase also exist, these can be driven in either bipolar or unipolar mode.

A pole can be defined as one of the regions in a magnetized body where the magnetic flux density is concentrated. Both the rotor and the stator of a step motor have poles. Figure 5 contains a simplified picture of a two-phase stepper motor having 2 poles (or 1 pole pairs) for each phase on the stator, and 2 poles (one pole pair) on the rotor. In reality several more poles are added to both the rotor and stator structure in order to increase the number of steps per revolution of the motor, or in other words to provide a smaller basic (full step) stepping angle. The permanent magnet stepper motor contains an equal number of rotor and stator pole pairs. Typically the PM motor has 12 pole pairs. The stator has 12 pole pairs per phase. The hybrid type stepper motor has a rotor with teeth. The rotor is split into two parts, separated by a permanent magnet, making half of the teeth south poles and half north poles. The number of pole pairs is equal to the number of teeth on one of the rotor halves. The stator of a hybrid motor also has teeth to build up a higher number of equivalent poles (smaller pole pitch, number of equivalent poles = $360/\text{teeth pitch}$) compared to the main poles, on which the winding coils are wound. Usually 4 main poles are used for 3.6 hybrids and 8 for 1.8- and 0.9-degree types.

It is the relationship between the number of rotor poles and the equivalent stator poles, and the number the number of phases that determines the full-step angle of a stepper motor.[9]

$$\text{Step angle} = 360 / (N_{\text{ph}} \cdot \text{Ph.}) = 360/N$$

N_{ph} = Number of equivalent poles per phase = number of rotor poles

Ph. = Number of phases

N = Total number of poles for all phases together

2.5.6 Stepper Motor Mechanical Parameters

The performance of a stepper motor system (driver and motor) is also highly dependent on the mechanical parameters of the load. The load is defined as what the motor drives. It is typically frictional, inertial or a combination of the two.

Friction is the resistance to motion due to the unevenness of surfaces which rub together. Friction is constant with velocity. A minimum torque level is required throughout the step in order to overcome this friction (at least equal to the friction). Increasing a frictional load lowers the top speed, lowers the acceleration and increases the positional error. The converse is true if the frictional load is lowered. Inertia is the resistance to changes in speed. A high inertial load requires a high inertial starting torque and the same would apply for braking. Increasing an inertial load will increase speed stability, increase the amount of time it takes to reach a desired speed and decrease the maximum self-start pulse rate. The converse is again true if the inertia is decreased.

The rotor oscillations of a stepper motor will vary with the amount of friction and inertia load. Because of this relationship unwanted rotor oscillations can be reduced by mechanical damping means however it is more often simpler to reduce these unwanted oscillations by electrical damping methods such as switch from full step drive to half step drive.[11]

2.6 Microcontroller

A microcontroller is a small computer on a single integrated circuit containing a processor core, memory, and programmable input/output peripherals, the chip also include program memory as shown in figure (3-8). Microcontrollers are designed for embedded applications, personal computers or other general purpose applications.

Microcontrollers are used in automatically controlled products and devices, such as automobile engine control systems, implantable medical devices, remote controls and other embedded systems. By reducing the size and cost compared to a design that uses a separate microprocessor, memory, and input/output devices, microcontrollers make it economical to digitally control even more devices and processes. Mixed signal microcontrollers are common, integrating analog components needed to control non-digital electronic systems [13].

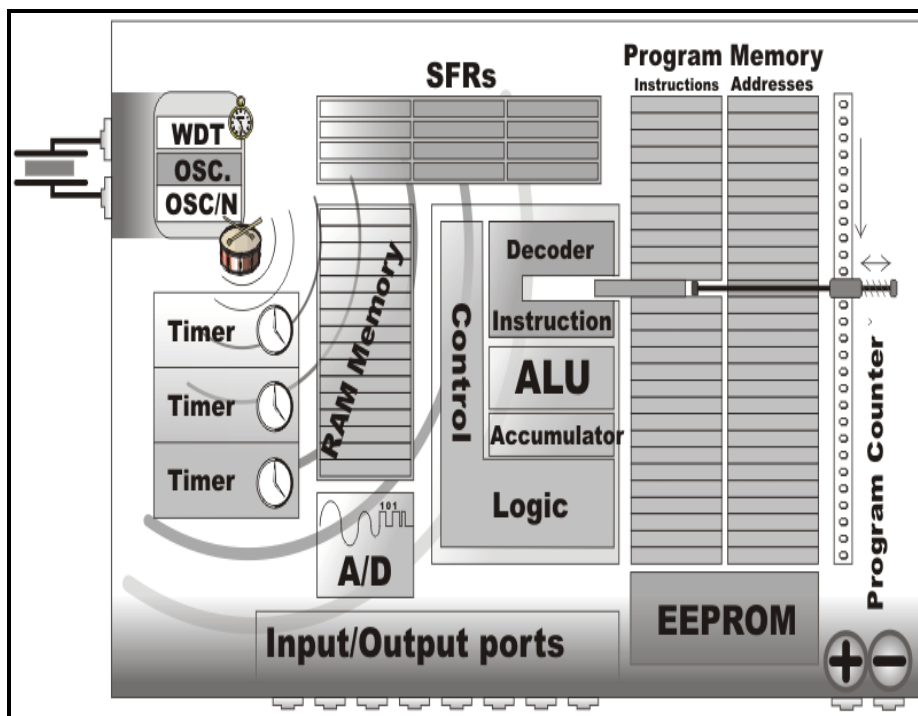


Figure (2.8): Structure of microcontroller^[13]

2.6.1 Types of microcontrollers

The microcontrollers are classified in terms of internal bus width, embedded microcontroller, instruction set, memory architecture, IC chip or VLSI core (VHDL or Verilog) file and family. For the same family, there may be various versions with various sources as in figure 2.9.

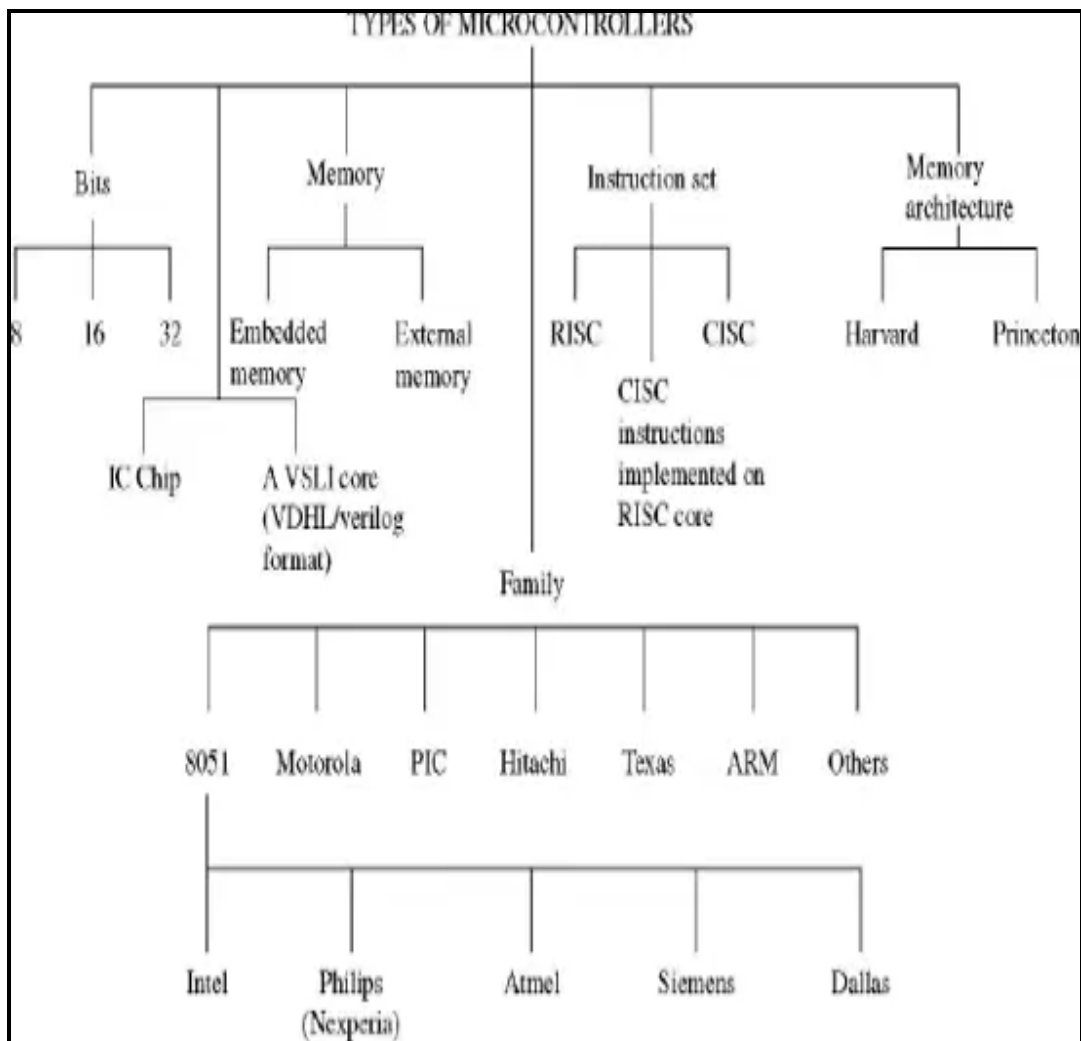


Figure (2.9) Type of microcontroller

I. The 8, 16 and 32-Bit Microcontrollers:

When an internal bus in an MCU is 8-bit bus and the ALU performs the arithmetic and logic operations on a byte at an instruction, the MCU is 8-bit microcontroller. Examples of 8-bit MCUs are Intel 8031/8051, PIC1x and Motorola MC68HC11 families.

When an internal bus in an MCU is 16-bit bus and the ALU performs arithmetic and logic operations on the operand words of 16 bits at the instructions, the MCU is 16-bit microcontroller. Important 16-bit MCUs are extended 8051XA, PIC2x, Intel 8096 and Motorola MC68HC12 families. 16-bit MCU provides greater precision and performance as compared to the 8-bit MCU.[15]

When an internal bus for the data transfer operations in an MCU is 32-bit bus and the ALU performs arithmetic and logic operations on operand words of 32 bits at the instructions, the MCU is 32-bit microcontroller. Important 32-bit MCUs are Intel/Atmel 251 family, PIC3x, Motorola M683xx and ARM 7 or 9 or 11 processor-based microcontroller families. These provide greater precision and performance compared to the 16-bit MCUs.

II. Embedded and External Memory Microcontrollers:

When an embedded system has an MCU that has all the hardware and software units in a single unit, the MCU is called embedded microcontroller. Very few or no other external unit or system is present for processing during the control or use of the external devices. For example, a telephone handset circuit uses an embedded microcontroller.

When an embedded system has an MCU that has all the hardware and software units present not as a single unit and has all or part of the memory unit externally interfaced using an interfacing circuit which is called the glue circuit, the MCU is called an external memory microcontroller. For example, 8031 has the program memory which is

interfaced externally to it. The 8051 has both internal as well as external program memory.

III. CISC and RISC Architecture Microcontrollers:

When an MCU has an instruction set that supports many addressing modes for the arithmetic and logical instructions and when there are the memory accesses during the ALU operations and the data transfer instructions, the MCU is said to be possessing CISC-architecture.

CISC provides flexibility in choosing various ways of performing the data transfer, arithmetic and other operations. For example, it is feasible to add contents of two registers or add the register and memory or add the bits at two memory addresses in a CISC. Instructions are of variable number of bytes in the CISC. These can take varying amounts of time interval for execution. An example is Intel 8096.

When an MCU has an instruction set that supports a few addressing modes for the arithmetic and logical instructions and just a few (load, store, push and pop) instructions for the data transfer, the MCU is said to be of RISC architecture. RISC provides no flexibility in choosing the many different ways of performing the arithmetic and logic operations. These operations are performed after the load of operands in the registers, and the results of these operations are placed in registers. The register contents are later on stored in the memory. RISC implements each instruction in a single cycle using a distinct hardwired control. It uses a lesser amount of circuitry. It has less power dissipation. There is reduced instruction set. Instructions are of fixed number of bytes and take a fixed amount of time for execution. It has many registers. Therefore, operations can be performed using them. The need for external fetches from the memories is greatly reduced. (An external fetch is to be done by the CPU for an operand more frequently in the CISC). The RISC provides a higher performance in computing than the

CISC. This is because little need of the external fetches, which takes a significant amount of processor time. High performance is also because of hardwired implementation of instructions. An example of RISC architecture is the ARM processor family-based MCU.

Most microprocessor and microcontroller designs are based on RISC core, because the CISC features can always be provided for programming with an appropriate on-chip compiler or internal circuit which translates the codes for the RISC core.

IV. Harvard and Princeton Memory Architecture

Microcontrollers:

When an MCU has a distinct memory address space for the program and data memory, the MCU has Harvard memory architecture in the processor. The MCU has separate instructions, and hence separate control signals, for the data transfers from these two memories. For example, 8051 has an address space between 0x0000 and 0xFFFF for the program memory bank and separate memory between 0x0000 and 0xFFFF for the data memory bank. (Bank saves the money; a memory bank saves the bytes during operations.)[14]

When an MCU has a common memory address space usable for the program memory and data memory, the MCU has Princeton memory architecture in the processor. For example, 68HC11 has an address space between 0x0000 and 0xFFFF for the program memory codes and the same space between 0x0000 and 0xFFFF for the data bytes. It has no separate instructions, and hence no separate control signals for data transfers from and to these two sets of memories. (Program and data can be stored on the same memory chip or unit within same address block).

2.6.3 Microcontroller operates:

A typical scenario on the basis of which it all functions is as follows:

- I. Power supply is turned off and everything is still, the program is loaded into the microcontroller, nothing indicates what is about to come.
- II. Power supply is turned on and everything starts to happen at high speed. The control logic unit keeps everything under control. It disables all other circuits except quartz crystal to operate. While the preparations are in progress, the first milliseconds go by.
- III. Power supply voltage reaches its maximum and oscillator frequency becomes stable. SFRs are being filled with bits reflecting the state of all circuits within the microcontroller. All pins are configured as inputs. The overall electronic starts operation in rhythm with pulse sequence. From now on the time is measured in micro and nanoseconds.
- IV. Program Counter is set to zero. Instruction from that address is sent to instruction decoder which recognizes it, after which it is executed with immediate effect. The value of the Program Counter is incremented by 1 and the whole process is repeated, several million times per second.

2.6.2 Atmel AVR

The AVR is a modified Harvard architecture 8-bit RISC single chip microcontroller which was developed by Atmel in 1996. The AVR was one of the first microcontroller families to use on-chip flash memory for program storage .as shown in table 2-1 AVR's are generally classified into many basic families in AVR, megaAVR, XMEGA [14].

Table (2.1): Different between basic families of AVR.

Basic families characteristics	InyAVR-the ATtiny series	Mega AVR- the ATmega series	XMEGA- the ATXMEGA series
program memory(KB)	0.5–16	4–512	16–384
pin package	6–32	28–100	44–64–100
peripheral set	Limited peripheral set	Extensive peripheral set	Extensive peripheral with DACs

2.6.3 ATmega32

The AT refers to Atmel the manufacturer, Mega means that the microcontroller belong to mega AVR category, 32 signifies the memory of the controller, which is 32KB.

The ATmega32 provides the following features: 512 bytes EEPROM, 2 Kbyte SRAM, 32 general purpose I/O lines, 32 general purpose working registers, three flexible Timer/Counters with compare modes, Internal and External Interrupts, a byte oriented ,Two-wire Serial Interface, an 8-channel, 10-bit ADC with optional differential input stage with programmable gain, A/D Converter^[17].

Following points explain the building blocks of Atmega32 architecture [16].

I. I/O Ports:

As show in figure 3-3 Atmega32 has four (PORTA, PORTB, PORTC and PORTD) an 8-bit bi-directional I/O port. Each bit called pin any of this pins has alternative function beside primary function.

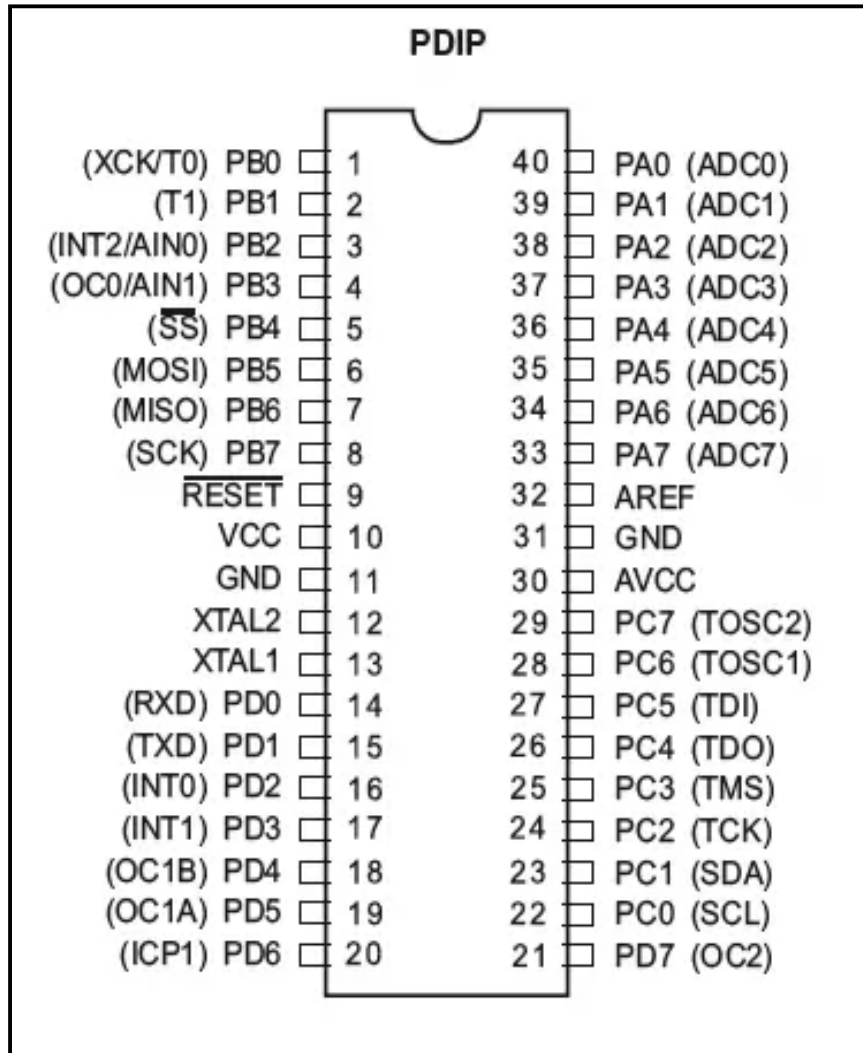


Figure (2.10) Pin description of ATMEGA32

II. Auxiliary Pin:

a. Voltage Common Cathode (VCC):

This pin provides digital supply voltage to the microcontroller.

b. Ground (GND):

This pin refers to circuit reference (Zero) voltage level.

c. RESET:

This pin use to make the microcontroller able to restart execution of the program.

d. Crystal clock Input 1(XTAL1):

This pin is an input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

e. Crystal clock Input 2(XTAL2):

This pin is an output from the inverting Oscillator amplifier.

f. Analog Collector Control Voltage (AVCC):

AVCC is the supply voltage pin for Port A and the A/D Converter. It should be externally connected to VCC, even if the ADC is not used. If the ADC is used, it should be connected to VCC through a low-pass filter.

g. Analog Reference (AREF):

AREF is the pin for the A/D Converter.

III. Internal Calibrated Oscillator:

Atmega32 is equipped with an internal oscillator for driving its clock. By default Atmega32 is set to operate at internal calibrated oscillator of 1 MHz the maximum frequency of internal oscillator is 8Mhz. Alternatively, ATmega32 can be operated using an external crystal oscillator with a maximum frequency of 16MHz. In this case you need to modify the fuse bits.

IV. ADC Interface:

Atmega32 is equipped with an 8 channel ADC with a resolution of 10-bits. ADC reads the analog input for e.g., a sensor input and converts it into digital information which is understandable by the microcontroller.

V. Timers/Counters:

Atmega32 consists of two 8-bit and one 16-bit timer/counter. Timers are useful for generating precision actions for e.g., creating time delays between two operations.

VI. Watchdog Timer:

Watchdog timer is present with internal oscillator. Watchdog timer continuously monitors and resets the controller if the code gets stuck at any execution action for more than a defined time interval.

VII. Interrupts:

Atmega³² consists of 21 interrupt sources out of which four are external. The remaining are internal interrupts which support the peripherals like USART, ADC, and Timers etc.

VIII. Universal Synchronous and Asynchronous Receiver and Transmitter interface (USART):

USART is available for interfacing with external device capable of communicating serially (data transmission bit by bit).

IX. General Purpose Registers:

Atmega16 is equipped with 32 general purpose registers which are coupled directly with the Arithmetic Logical Unit (ALU) of Control processing unit (CPU).

X. Memory:

Atmega³² consist of three different memory sections:

a. Flash EEPROM:

Flash EEPROM or simple flash memory is used to store the program dumped or burnt by the user on to the microcontroller. It can be easily erased electrically as a single unit. Flash memory is non-volatile i.e., it retains the program even if the power is cut-off. Atmega³² is available with 32KB of in system programmable Flash EEPROM.

b. Byte Addressable Electronic Erasable Programmable Read-Only Memory (EEPROM):

This is also a nonvolatile memory used to store data like values of certain variables. Atmega16 has 1024 bytes of EEPROM; this memory can be useful for storing the lock code if we are designing an application like electronic door lock.

c. Static Random Access Memory (SRAM):

SRAM, this is the volatile memory of microcontroller i.e., data is lost as soon as power is turned off. Atmega32 is equipped with 4KB of internal SRAM. A small portion of SRAM is set aside for general purpose registers used by CPU and some for the peripheral subsystems of the microcontroller.

X. In System Programming(ISP):

AVR family of controllers have ISP Flash Memory which can be programmed without removing the IC from the circuit, ISP allows to reprogram the controller while it is in the application circuit.

XI. Serial Peripheral Interface (SPI):

SPI port is used for serial communication between two devices on a common clock source. The data transmission rate of SPI is more than that of USART.

XII. Two Wire Interface (TWI):

TWI can be used to set up a network of devices, many devices can be connected over TWI interface forming a network, the devices can simultaneously transmit and receive and have their own unique address.

XIII. Digital to Analog Converter (DAC):

Atmega16 is also equipped with a DAC interface which can be used for reverse action performed by ADC. DAC can be used when there is a need of converting a digital signal to analog signal.

XIV. Special function registers:

It is a registers within a microcontroller, which controls or monitors various aspects of the microcontroller's function. Depending on the microcontroller architecture:

a. Data Direction Register (DDR):

The data direction register composed of four registers (DDRA, DDRB, DDRC and DDRD), it programmed to select whether each individual input/output pin is configured as an input or an output.

b. ADC Multiplexer Register (ADMUX):

This register used to select ADC Voltage Reference and controls which of the eight possible inputs are being activated.

c. ADC Control and Status Register (ADCSRA):

This register controls the functioning of the ADC (enable ADC, start conversation, etc.).

d. Analog to Digital Word (ADCW):

This register is ADC data register and it split into ADCH/ADCL registers which allows retrieving the data from the ADC result registers.

e. Timer/Counter Control register (TCCR1):

This register is control register for Timer 1; it is actually composed of two registers TCCR1A and TCCR1B which used to set the timer mode, pre scalar and other options.

f. Timer/Counter(TCNT0):

This register is used to hold counting values .It is a 8 bit register and it can hold up to 255(0XFF).

g. Output Compare Register (OCR1) :

This register composed of two registers OCR1A (which splits into OCR1AL/OCR1AH) and OCR1B (which splits into OCR1BL/OCR1BH).The content of the register is continuously

Compared with TCNT0 content; if both are equal it can be used to generate compare match interrupt to occur or waveform generation.

h. Input Capture Register (ICR1) :

This register is split into ICR1L /ICR1H registers, it contains the maximum timer count to which the OCR1 compare to obtain PWM period.

i. Analog Comparator Control and Status Register(ACSR) :

This is used to control the analog comparator functions.

j. Special Function IO Register (SFIOR):

This register used to reset pre scalar.

2.7 Real time embedded system

2.7.1 Overview of embedded systems

An embedded system is a specialized computer system that is part of a larger system or machine. Embedded systems can also be thought of as information processing subsystems integrated in a larger system. As part of a larger system it largely determines its functionality. An embedded system usually contains an embedded processor. Many appliances that have a digital interface -- microwaves, VCRs, cars -- utilize embedded systems. Some embedded systems include an operating system. Others are very specialized resulting in the entire logic being implemented as a single program. These systems are embedded into some device for some specific purpose other than to provide general purpose computing [12]

Embedded systems provide several functions

- Monitor the environment; embedded systems read data from input sensors. This data is then processed and the results displayed in some format to a user or users

- Control the environment; embedded systems generate and transmit commands for actuators.
- Transform the information; embedded systems transform the data collected in some meaningful way, such as data compression/decompression

Embedded systems typically execute applications such as control laws, finite state machines, and signal processing algorithms. These systems must also detect and react to faults in both the internal computing environment as well as the surrounding electromechanical systems.

There are many categories of embedded systems, from communication devices to home appliances to control systems. Examples include;

- Communication devices , modems, cellular phones
- Home Appliances , CD player, VCR, microwave oven
- Control Systems , Automobile anti-lock braking systems, robotics, satellite control

2.7.1.1 Characteristics of Embedded Systems

Embedded systems are characterized by a unique set of characteristics. Each of these characteristics imposed a specific set of design constraints on embedded systems designers. The challenge to designing embedded systems is to conform to the specific set of constraints for the application. The characteristics are as the following:

Application Specific Systems

Reactive Systems

Distributed Systems

Heterogeneous Architectures

Harsh environment

System safety and reliability

Control of physical systems

Small and low weight

Cost sensitivity

Power management

2.7.1.2 Requirements for Embedded Systems

Embedded systems are unique in several ways, as described above. When designing embedded systems, there are several categories of requirements that should be considered;

- Functional Requirements
- Temporal Requirements (Timeliness)
- Dependability Requirements

Functional Requirements

Functional requirements describe the type of processing the system will perform. This processing varies, based on the application. Functional requirements include the following;

- Data Collection requirements
- Sensing requirements
- Signal conditioning requirements
- Alarm monitoring requirements
- Direct Digital Control requirements
- Actuator control requirements

- Man-Machine Interaction requirements (Informing the operator of the current state of a controlled object for example. These interfaces can be as simple as a flashing LED or a very complex GUI-based system. They include the ways that embedded systems assist the operator in controlling the object/system. [12])

Temporal Requirement

Embedded systems have many tasks to perform, each having its own deadline. Temporal requirements define the stringency in which these time-based tasks must complete.

Temporal requirements can be very tight (for example control-loops) or less stringent (for example response time in a user interface).

Dependability Requirements

Most embedded systems also have a set of dependability requirements

Reliability; this is a complex concept that should always be considered at the system rather than the individual component level. There are three dimensions to consider when specifying system reliability; Hardware reliability; probability of a hardware component failing o Software reliability; probability that a software component will produce an incorrect result

Operator reliability; how likely that the operator of a system will make an error.

There are several metrics used to determine system reliability;

Probability of failure on demand; likelihood that the system will fail when a service request is made. Rate of failure occurrence; frequency of

occurrence with which unexpected behavior is likely to occur. Mean Time to Failure; the average time between observed system failures.

Safety: describe the critical failure modes and what types of certification are required for the system

Maintainability: describes constraints on the system such as type of Mean Time to Repair (MTTR).

Availability: the probability that the system is available for use at a given time.

Security: these requirements are often specified as “shall not” requirements that define unacceptable system behavior rather than required system functionality. [12]

2.7.2 Overview of real-time systems

A real-time system is a system that is required to react to stimuli from the environment (including the passage of physical time) within time intervals dictated by the environment. The Oxford dictionary defines a real-time system as “Any system in which the time at which output is produced is significant”. This is usually because the input corresponds to some movement in the physical world, and the output has to relate to that same movement. The lag from input time to output time must be sufficiently small for acceptable timeliness. Another way of thinking of real-time systems is any information processing activity or system which has to respond to externally generated input stimuli within a finite and specified period. Generally, real-time systems are systems that maintain a continuous timely interaction with its environment [12]

Correctness of a computation depends not only upon its results but also upon the time at which its outputs are generated a real-time system must satisfy bounded response time constraints or suffer severe consequences. If the consequences consist of a degradation of performance, but not failure, the system is referred to as a soft real-time system (e.g. time adjusting system on computers over the network) If the consequences are

system failure, the system is referred to as a hard real-time system. (E.g. emergency patient management system in hospitals).

There are two types of real-time systems: reactive and embedded. Reactive real-time system involves a system that has constant interaction with its environment. (e.g. a pilot controlling an aircraft). An embedded real-time system is used to control specialized hardware that is installed within a larger system. (e.g. a microprocessor that controls the fuel-to-air mixture for automobiles).

Real time is a level of computer responsiveness that a user senses as sufficiently immediate or that enables the computer to keep up with some external process (for example, to present visualizations of the weather as it constantly changes). Real-time is an adjective pertaining to computers or processes that operate in real time. Real time describes a human rather than a machine sense of time. [12]

Examples of real-time systems include;

- Software for cruise missile
- Heads-up cockpit display
- Airline reservation system
- Industrial Process Control
- Banking ATM

Real-time systems can also be found in many industries;

- Defense systems
- Telecommunication systems
- Automotive control
- Signal processing systems
- Radar systems

- Automated manufacturing systems
- Air traffic control •Satellite systems
- Electrical utilities

2.7.2.1Real-Time Event Characteristics

Real-time events fall into one of the three categories: asynchronous, synchronous, or isochronous.

- Asynchronous events are entirely unpredictable. For example, the event that a user makes a telephone call. As far as the telephone company is concerned, the action of making a phone call cannot be predicted.
- Synchronous events are predictable and occur with precise regularity if they are to occur. For example, the audio and video in a movie take place in synchronous fashion.

Isochronous events occur with regularity within a given window of time. For example, audio bytes in a distributed multimedia application must appear within a window of time when the corresponding video stream arrives. Isochronous is a sub-class of asynchronous [12]

2.8Previous Study

Proportion to the importance of research under study (control of parabolic reflector antenna parameters(gain)) many researcher and case studies have been done in this side to obtain optimum solution for any problem have affected of transmission lines quality .The main objective of parabolic reflector antenna Is introduce radiation with high quality and that is means the transmit and receive signal is very good because the gain of parabolic refactor antenna is characterized as high gain which is favored it over the rest of antenna to be used at microwave and

any transmission link for long distance as radar, satellite and telecom fields

Most of previous studies about enhancement of parabolic reflector antenna gain and helical antenna gain are theoretical methods depend upon analysis for basic equation and calculation and there are some procedure follow the simulation methods to get optimum results to contribute for further searching .Here in this paragraph more than 25 paper have been check to find out the previous procedure and cases studies to bring new research which contribute at research side

As R.Heerasings [22] take the case study of parabolic reflector antenna control to get optimum gain and received signal .The research activities involves to design and modeling concept of drive control system for antenna reflector including1 implementing ,testing and commissioning of ground station antenna for remote sensing satellite tracking. The field of research involves integration and establishment of drive chains for elevation and azimuth axes of antenna, optimization tuning of entire integrated system with use of approximation obtained from mathematical modeling and simulation studies. The method of this research depend upon mathematical equation calculation and mat lab simulation which is get approximate results and graphs . At the conclusion the study have a good result according to mathematical modeling and mat lab simulation to movement the antenna body at two axes as elevation angle and azimuth angel.

Myeongkyum [23] the researcher discussed in paper the precise Attitude Control System Design for the Tracking of Parabolic Satellite Antenna. The Satellite antenna is parabolic reflector antenna which it has high gain .In this study the researcher concern of control the movement of antenna at Azimuth angle and elevation angle by using BLAD for fast response .In order to solve the various communication errors such as moving antenna or ground the researcher design control system. Experiment have been done and it have good result but the result of received signal have short noise regarding BLDC usage and there should

be more research to support it

On the other hand Ode week [24] presents a research on the adaptive technique for radiation pattern shaping of parabolic antenna. The procedure of research is to control the shape of parabolic center feed reflector designed for carrier frequency of 12 GHz. The main issue is to get High gain of radiation pattern by change the location of feeder center at parabolic reflector antenna using the shape Memory Alloy (SMA) wire movement. The movement of wire change the location of the feeder of reflector antenna according to thermodynamically model of actuator. At the end the result has been shown that the reflector surface can be shaped with the help of SMA actuators acting on the mesh periphery. This shape change affect the far-field radiation pattern.

From the side of helical antenna parameters improvement and control there are many research have been done. Here some research on this part will discuss, ShiQ [5] the research discussed the optimization design of helical antenna that the optimization concerned of helical antenna gain. The optimization design of the antenna is that its input impedance matching has been improved by adjusting the copper strip matching stub, while its circular polarization by performance has been enhance by changing the parasitic radiation path loaded in the front of the antenna. The optimal antenna structure for INMARSAT application has been fabrication and measured. This antenna can produce gain of higher than 9 dB. At the end of research the conclusion points that the circular polarization radiation performance of the antenna can be optimized by changing the parasitic radiation patch, and then the impedance can be tuned to coincide with axial ratio bandwidth by changing the copper strip matching stub. The antenna has characterized of high light weight, low profile and easy tuning. These characterized make this antenna

especially suitable for small size and high gain antenna

Mohamed [26] have case study of design, assembly and field testing of LHCP (left hand circularly polarization) high gain helical antenna. The antenna is to be utilized for the reception or reflected Global Position System (GPS) signal .The major design parameter was obviously high gain while maintain the polarization integrity of reflected GPS signals .The research methodology is carried out calculation for helical antenna parameters especially the wave length, no of turn and space between turn to get the optimum value that get high gain .At the end of research the instructor recommend for more studies for this antenna which is widely application for high gain antennas and for left hand circularly polarization at satellite communication

B.Venkateshwar [27] the researcher design and optimization of helical antenna used as transmitting end of GPS in L band .The first phase of optimization is focused upon driving designing that is based on the govern equation of helical antenna and simulation and functional verification is don using HFSS (high Frequency structure simulator)and made a necessary change to give rise to a model for design optimization .In second phase the helix antenna model is optimize for different parameters like number of turn diameter of the ground plate and observe the radiation pattern of helical antenna

Also there are research at stepper motor side which is auxiliary part of our research when Emad d A [28] discussed the general relationship between step-angle of the stepper motor and the satellite dish antenna diameter and beam-width. This relationship insures that the dish antenna directed within the HPBW when it position to any satellite within the rang. Mathematical and calculation procedure have been follow to get the relation .the conclusion of study is From the results we can say that the step-angle of the stepper motor limits the diameter of the

antenna that can be used when we connect them directly and vice-versa. Connecting motor using gear to the antenna lets the design more flexible. By this way we can use stepper motor with less resolution and adjusting resolution of antenna step-angle by calculating the optimum gear- ratio (base on the HPBW and antenna diameter).

Chapter Three

System Design

3.1 Hardware design

The hardware design of the system is based on using a microcontroller as a processor. Interface circuits are connected to the microcontroller. A matrix keypad is connected to the microcontroller for data entry. An LCD is connected to a port of the microcontroller to display data. Four stepper motors are connected to the interface circuit in order to control the four sectors of the parabolic reflector of the antenna. A stepper motor is connected to the interface circuit in order to control the helix feed of the antenna. Figure (3.1) shows the block diagram of the system design and Figure (3.2) describes the circuit connection

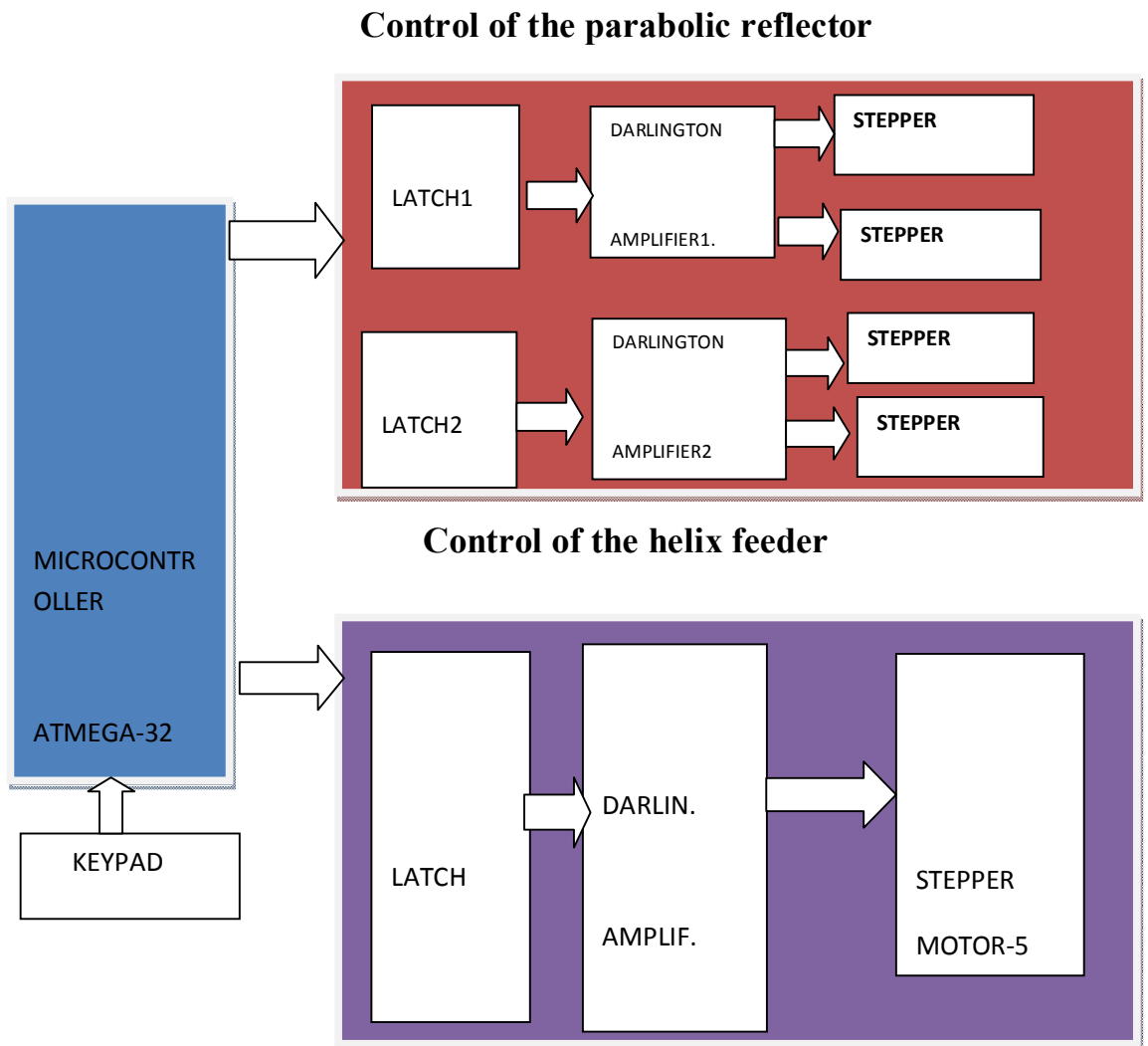


Figure (3.1) block diagram for parabolic reflector antenna control

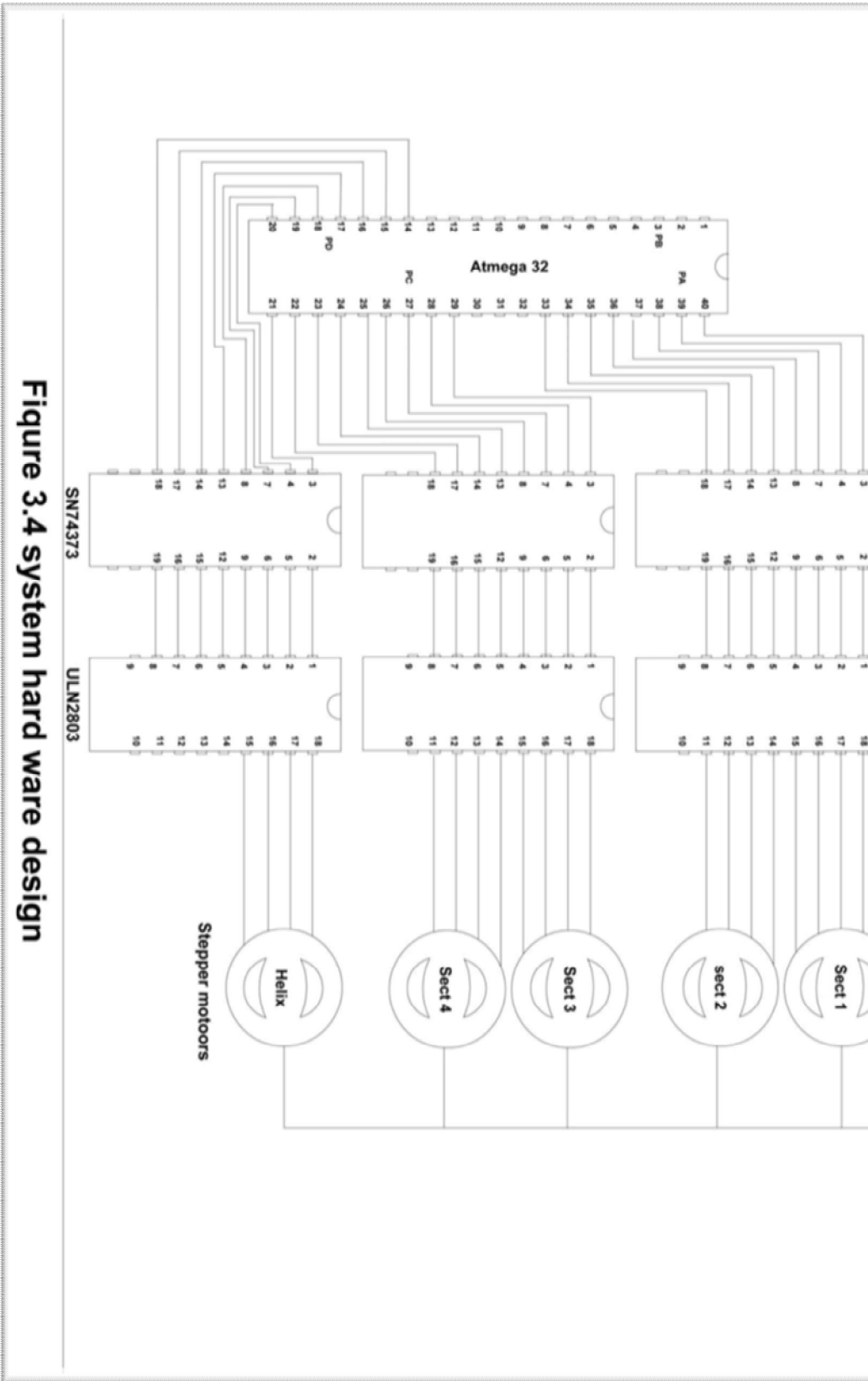


Figure 3.4 system hard ware design

3.1.1 Hardware system component

3.1.1.1 Personal computer (PC):

PC computer is used for programming the microcontrollers.

3.1.1.2 Microcontroller :

Atmega 32 microcontroller will be used as a means of control of the stepper motors. The Microcontroller (ATMEGA32) is already simulated in proteus program as illustrate in Figure3-3. The microcontroller read signal through port B to convert it form analog signal to digital signal. After that the microcontroller process data and output is easily taken from the port determined in the code (A, C, D). Microcontroller needs 5V to work properly.

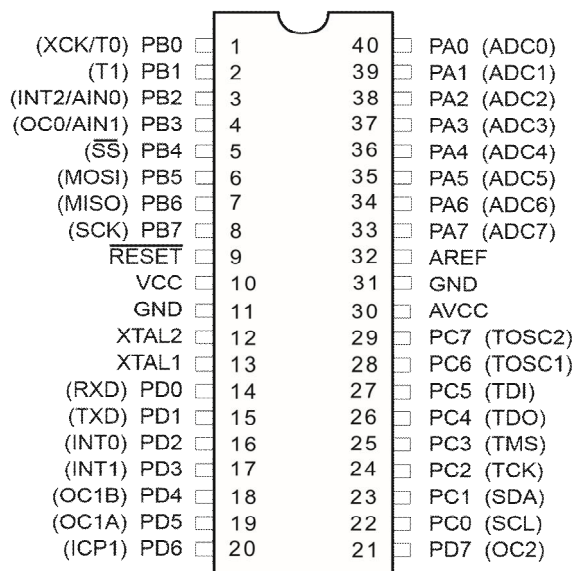


Figure (3.3) Atmeg32 pin description

3.1.1.2.1 ATMEGA 32 port description

Port A (PA7...PA8)

Port A serves as the analog inputs to the A/D convertor

Port A also serves as an 8-bit bi-directional I/O port, if the A/D Converter is not used. Port pins can provide internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability. When pins PA0 to PA7 are used as inputs and are externally pulled low, they will source current if the internal pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running

Port B (PB7...PB8)

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B also serves the functions of various special features of the ATmega32.

Port C (PC7...PC8)

Port C is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port

C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running. If the JTAG interface is enabled, the pull-up resistors on pins PC5 (TDI), PC3 (TMS) and PC2 (TCK) will be activated even if a reset occurs.

The TD0 pin is tri-stated unless TAP states that shift out data are entered.

Port C also serves the functions of the JTAG interface and other special features of the ATmega32 as listed on page 60.

Port D (PD7...PD8)

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port D also serves the functions of various special features of the ATmega32 as listed on page 62.

ATMEGA 32 Pin description

h. Voltage Common Cathode (VCC):

This pin provides digital supply voltage to the microcontroller.

i. Ground (GND):

This pin refers to circuit reference (Zero) voltage level.

j. RESET:

This pin use to make the microcontroller able to restart execution of the program.

k. Crystal clock Input 1(XTAL1):

This pin is an input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

l. Crystal clock Input 2(XTAL2):

This pin is an output from the inverting Oscillator amplifier.

m. Analog Collector Control Voltage (AVCC):

AVCC is the supply voltage pin for Port A and the A/D Converter. It should be externally connected to VCC, even if the ADC is not used. If the ADC is used, it should be connected to VCC through a low-pass filter.

n. Analog Reference (AREF):

AREF is the pin for the A/D Converter.

Figure (3.4) illustrate the block diagram of microcontroller at mega 32 which contain the internal and external communication with microcontroller

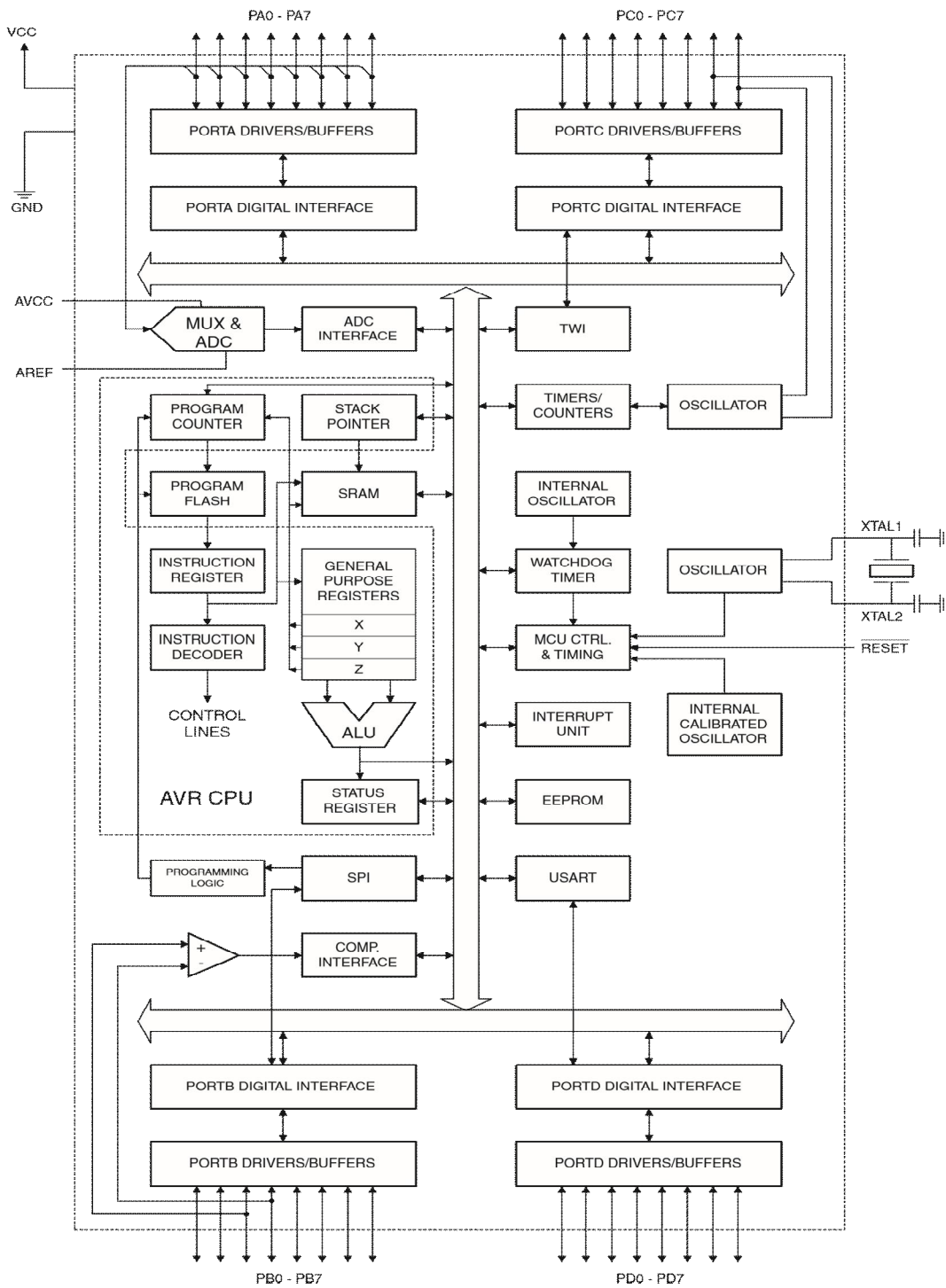


Figure (3.4) block diagram of atmega32

31.1.3 HD74LS373 Latching IC:

The HD74LS373, 8-bit register features totem-pole three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide this register with the capacity of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was setup. The (IC) layout is shown in figure (3.5) below

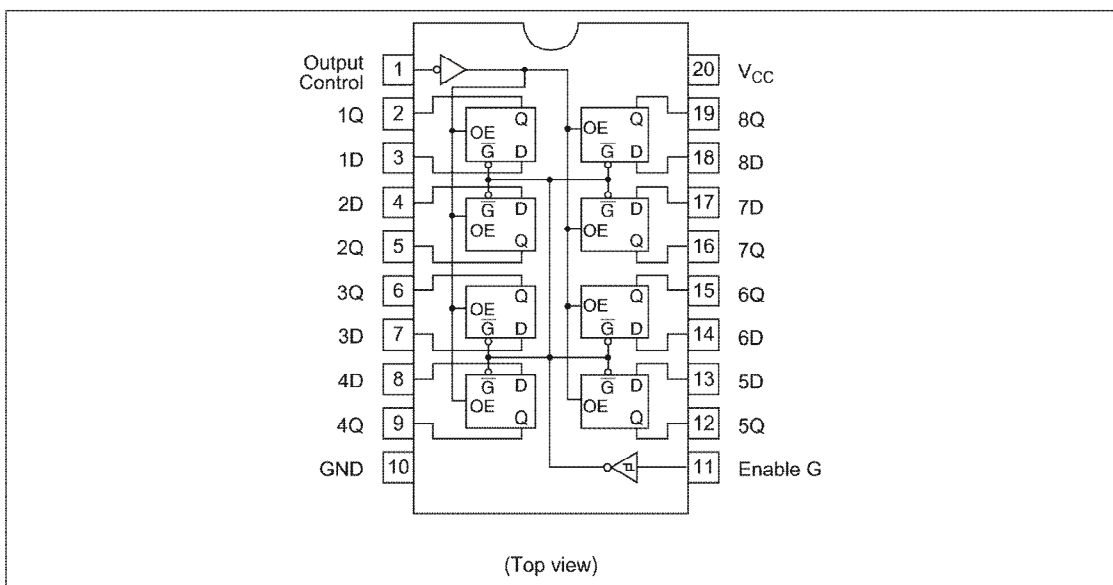


Figure (3.5) HD74LS373

Table (3.1) Recommended Operating Conditions of HD74LS373

Item	Symbol	Min	Typ	Max	Unit	
Supply voltage	V_{CC}	4.75	5.00	5.25	V	
Output voltage	V_{OH}	—	—	5.5	V	
Output current	I_{OH}	—	—	-2.6	mA	
	I_{OL}	—	—	24	mA	
Operating temperature	T_{opr}	-20	25	75	°C	
Enable pulse width	"H" Level	t_w	15	—	—	ns
	"L" Level		15	—	—	ns
Data setup time	t_{su}	5↓	—	—	ns	

3.1.1.4ULN 2803A Darlington IC:

The ULN2803A is a high-voltage, high-current Darlington transistor array. The device consists of eight NPN Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of each Darlington pair is 500 mA. The Darlington pairs may be connected in parallel for higher current capability applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers. The ULN2803A has a 2.7-k Ω series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS devices. The (IC) layout is shown in figure (3.6) and figure (3.7) there is internal described for each pin

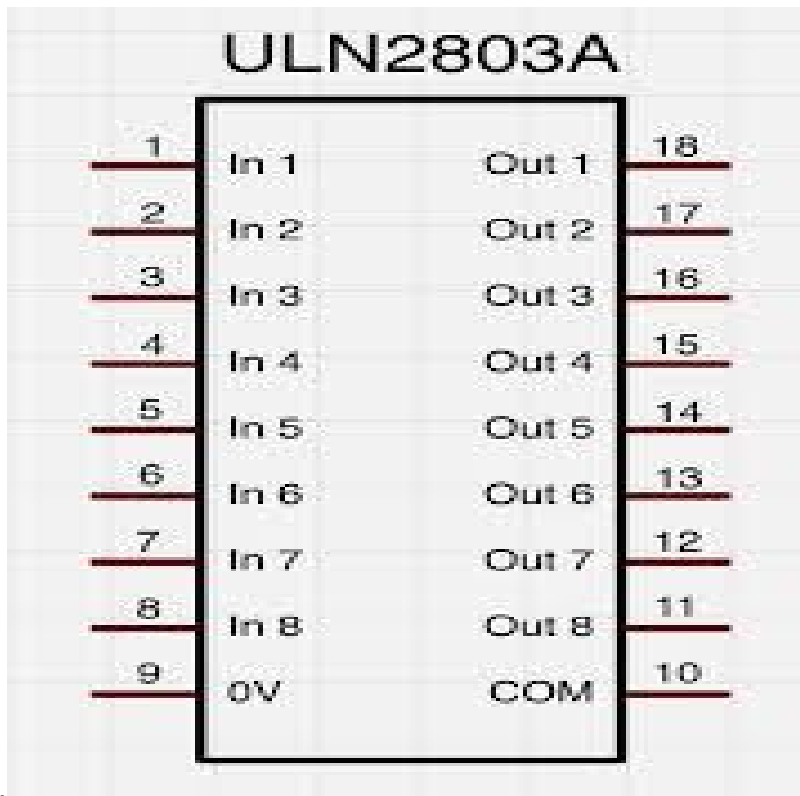


Figure (3.6) ULN 2803A

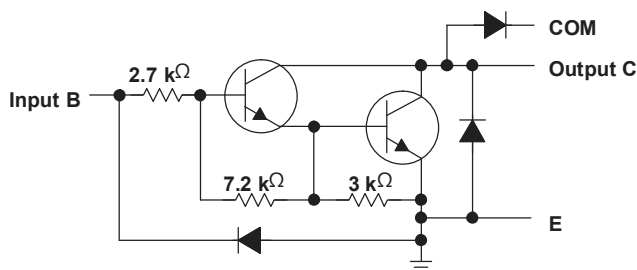


Figure (3.7) Schematic (each Darlington pair)

3.1.1.5 Stepper motor:

A five wires stepper motors will be used .One wire is for power supply to the stepper motor and the other four wires are connected to the windings of the stepper motor.

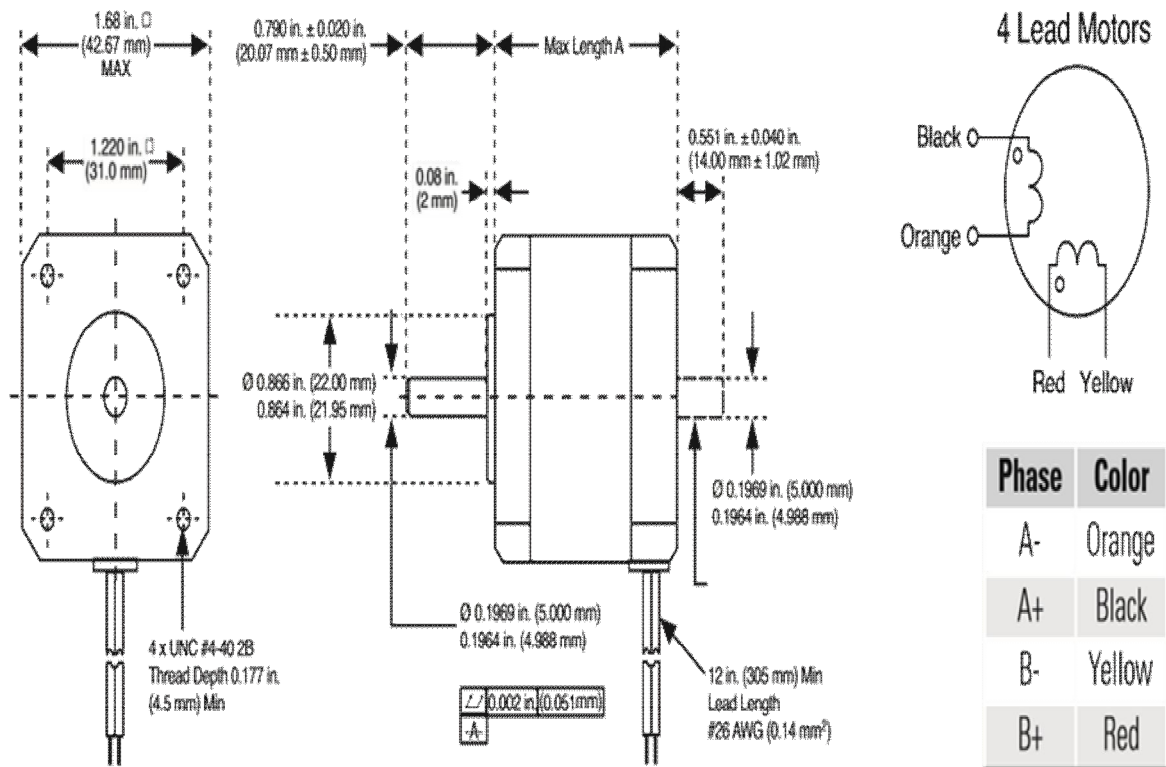


Figure (3.8) stepper motor dimension and terminal

Figure (3.8) shows the stepper motor devices dimension and the colour code of stepper motor wire

General identification for stepper motor:

Amps/phase – The maximum amount of current allowed through a phase of the stepper motor. Holding torque, the speed versus

torque curve, and so on is determined when the motor is excited by this value. The specifications listed in this data sheet are adjusted for the winding configuration.

Angular accuracy – A percentage of the step angle that defines the accuracy of each full step.

Detent torque (cogging torque) – The amount of torque necessary to rotate the stepper motor one full step when the motor is reenergized.

Differential line driver – A type of electrical digital output that can transmit digital data over a long distance. It consists of a complementary pair of digital lines. Electrical symmetry – How close each quadrature channel is to a 50 percent duty cycle when at a constant speed.

holding torque – The amount of torque necessary to rotate the stepper motor one full step (micro stepping turned off) when the motor is energized at the rated amps/phase of that motor. Minimum edge separation – Defines in degrees how close (electrically) an edge on channel A can be to an edge on channel B.

Phase inductance – The inductance of each phase of the stepper motor. The specifications listed in this data sheet are already adjusted for the winding configuration.

Phases – A wound wire in the stepper motor that is excited with current to produce electromagnetic force. Two or more phases work together by alternating between positively energized, reenergized, and negatively energized states to rotate the

stepper motor. Quadrature phasing – The electrical phase shift between channels A and B in a quadrature encoder. step angle – The distance the motor rotates each full step of the stepper motor. Also defined as 360 degrees divided by the steps per revolution.

3.1.1.6 Twelve keys matrix keypad:

The keypad supplies the Atmega 32 microcontroller with the number of step angles required to rotate the stepper motors.

The 12 keys keypad is widely used in many applications, some of those are: telephones and ATM machines. There are many different types of keypads and the keypad which would be explained here would be a matrix method in order to find which key is pushed. This keypad does not have pins for Vdd or Vgnd, which means it, does not require a direct connection to a voltage source to perform its task. Also this keypad has 7-pins and each pin would represent a row or a column. As this keypad has 12 keys, it has 3 columns and 4 rows. The mount of the keypad is as seen in figure (3.10), which shows the dimension and pins location. Moreover, the matrix of the keys related to pins is shown in figure (3.9). Those Figures are important in order to understand how the keypad is built, and how it would be used. Also, they show important information that is needed to understand the pin layout and the calibration between each key and its two pins.

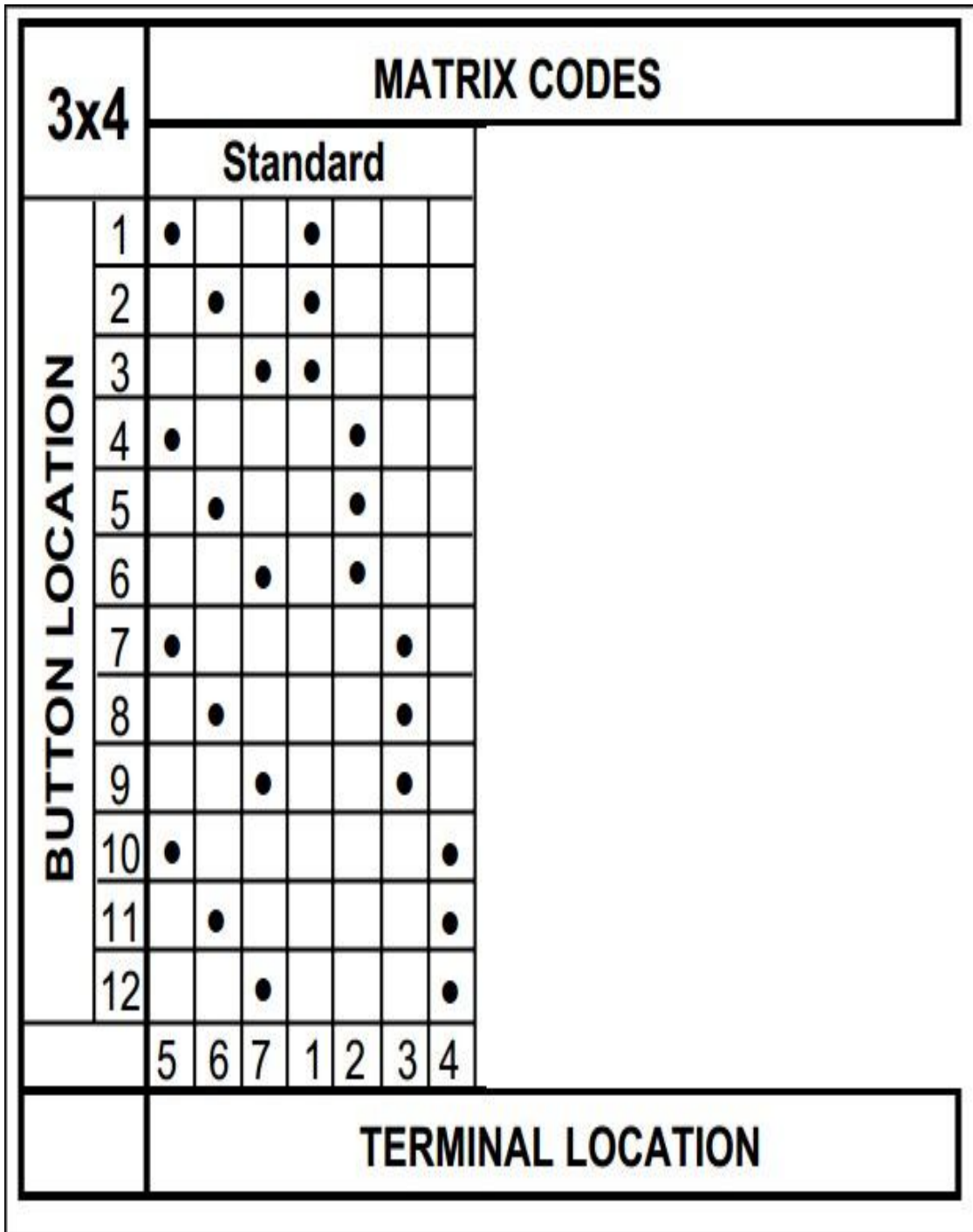


Figure (3.9) matrix keypad

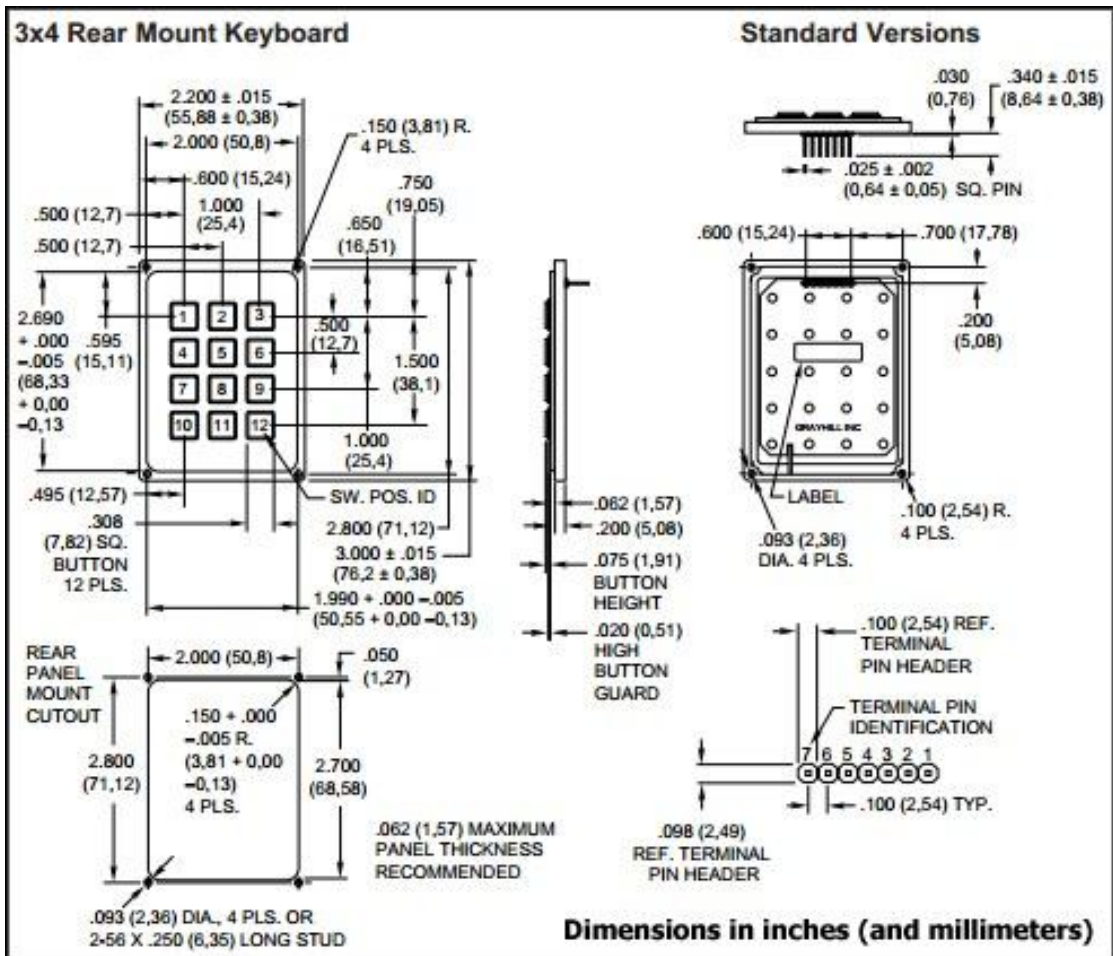


Figure (3.10) Keypad dimension illustration

Keypad properties:

The keypad has a 3-columns and 4-rows matrix orientation as seen in figure 2. If a key is pushed then the circuit would be shorted for those specific key pins. The short circuit would always be between a row pin and a column pin. For this specific 96AB2-152-F keypad the rows 1-4 are represented by pins 1-4 and columns 1-3 are represented by pins 5-7. For example button 1 would be represented by pins 1 and 5, so if a voltage is

applied to one of the pins and a voltammeter is connected to the other pin, when the button is pushed the voltammeter would read the input voltage. From Figure (3.9) it would be easy to construct a table that would show each button represents what character, and which pins are shorted if that button is pressed, which is provided in Table 1

Table (3.2) twelve keypad button representation

Key Number	Character	Culomn Pin	Row Pin
1	'1'	5	1
2	'2'	6	1
3	'3'	7	1
4	'4'	5	2
5	'5'	6	2
6	'6'	7	2
7	'7'	5	3
8	'8'	6	3
9	'9'	7	3
10	'*'	5	4
11	'0'	6	4
12	'#'	7	4

3.1.1.7 LCD:

LCD is used to display the data entry and the real time data during the system processing .Figure (3.11) shows the LCD photo



Figure (3.11) LCD

LCD-Liquid Crystal Display is an electronic device for displaying text or characters. We are using 14 pin LCD. 16*2 represents 16 characters and 2 line display. LCD's are economical and easily programmable and can easily display special and custom characters.

Pin description is as follows

1. Pin 7 to pin 14-All 8 pins are responsible for the transfer of data.
2. Pin 4-This is RS i.e., register select pin.
3. Pin 5-This is R/W i.e., Read/Write pin.
4. Pin 6-This is E i.e., enable pin.
5. Pin 2-This is VDD i.e., power supply pin.
6. Pin 1-This is VSS i.e., ground pin.
7. Pin 3-This is short pin

3.2 Software Design

The software design is performed by programming the main controller circuit (atmega32) which is connected to an interface circuit designed to drive the stepper motors, .The software package used here is BASCOM. BASCOM is an Integrated Development Environment (IDE) that supports the 8051 family of microcontrollers and some derivatives as well as Atmel's AVR microcontrollers. Two products are available for the various microcontrollers –BASCOM8051 and BASCOM-AVR

BASCOM-8051 BASCOM-AVR are development environments build around a powerful BASIC compiler which is suited for project handling and program development for the 8051 family and its derivatives as well as for the AVR microcontroller for Atmel

Figure (3.12) shows the interconnection for programming the microcontroller.

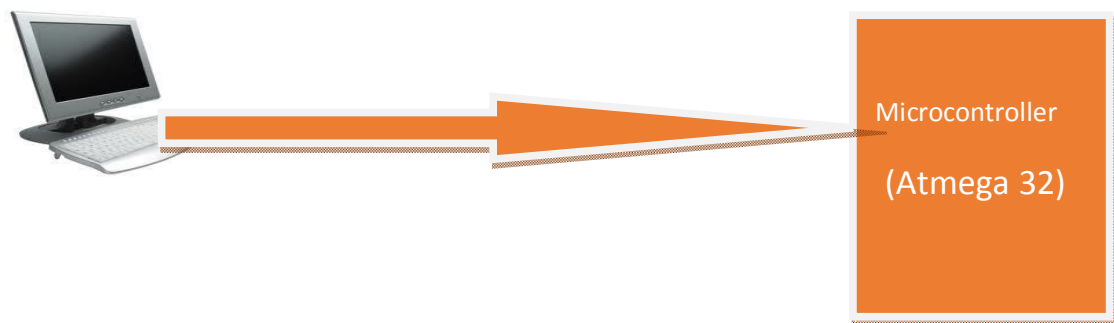


Figure (3.12) lab link cable

The system design includes five stepper motors divided into two parts. Part one is concerned with the control of the parabolic reflector while part two controls the helix feeder of the antenna .In part one; each stepper motor controls a sector of (90 degrees) of the parabolic antenna. In part two, the stepper motor control the helix feeder of the parabolic antenna.

3.2.1 System Algorithm

The algorithm is:

Start

- Initialization :

- Put all stepper motors at initial state.
 - Wait for an input from the keypad.

--- Enter data from the keypad:

- Enter the number of steps for stepper motor-1.
- Enter the number of steps for stepper motor-2.
- Enter the number of steps for stepper motor-3.
- Enter the number of steps for stepper motor-4.
- Enter the number of steps for stepper motor-5.
- If the (address = *) , Go to end of program.

--- Check the addresses of the stepper motors:

- If the (address = 1) , call subroutine of stepper motor-1.
- If the (address = 2) , call subroutine of stepper motor-2.
- If the (address = 3) , call subroutine of stepper motor-3.
- If the (address = 4) , call subroutine of stepper motor-4.
- If the (address = 5) , call subroutine of stepper motor-5.

--- Go to enter data from the keypad.

--- End.

--- Subroutine of stepper motor-1:

- Apply calculations to specify the number of step angles required.

- Rotate the stepper motor one step.

- Wait for few seconds.

- Decrement the number of steps.

- If the number of steps becomes zero, terminate the subroutine.

--- Return.

--- Subroutine of stepper motor-2:

- Apply calculations to specify the number of step angles required.

- Rotate the stepper motor one step.

- Wait for few seconds.

- Decrement the number of steps.

- If the number of steps becomes zero, terminate the subroutine.

--- Return.

--- Subroutine of stepper motor-3:

- Apply calculations to specify the number of step angles required.

- Rotate the stepper motor one step.

- Wait for few seconds.

- Decrement the number of steps.
- If the number of steps becomes zero, terminate the subroutine.

--- Return.

--- Subroutine of stepper motor-4:

- Apply calculations to specify the number of step angles required.

- Rotate the stepper motor one step.
- Wait for few seconds.
- Decrement the number of steps.
- If the number of steps becomes zero, terminate the subroutine.

--- Return.

--- Subroutine of stepper motor-5:

- Apply calculations to specify the number of step angles required.

- Rotate the stepper motor one step.
- Wait for few seconds.
- Decrement the number of steps.
- If the number of steps becomes zero, terminate the subroutine.

--- Return.

Chapter Four

Results and Discussion

4.1 Overview

Many simulation and calculation have been conducted regarding parabolic reflector antenna parameters and helical antenna parameters to configure and forecasting the research results to get optimum values. Based on the results of calculation obtained, a program was written.

4.2 Parabolic Reflector Antenna Parameters Configuration Simulation Results

Calculated parameters are simulated by using ICARA (Induced Current Analysis of Reflector antenna) software tool .The behavior of reflector antenna is prepare using Physics Optics method. The maximum reflector antenna gain and the maximum efficiency are found by taking the most appropriate F/D ratio as shown in the figures (4.1, 4.2 and 4.3)

In figure (4.1) the reflector configuration of the proposed antenna is shown and the input parameters are placed as main dish diameter and focal length

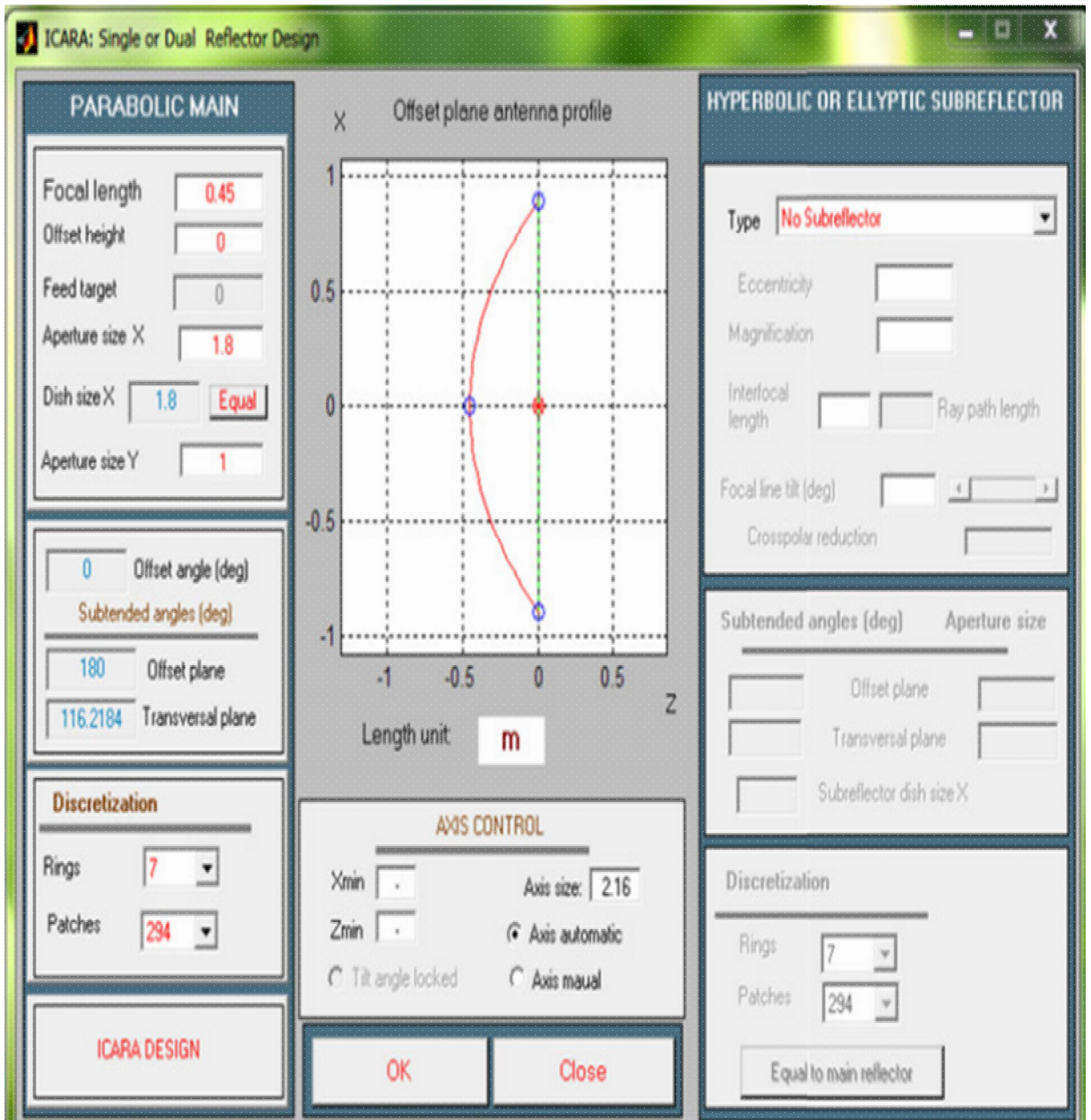


Figure (4.1) Parabolic Reflector Antenna Configuration

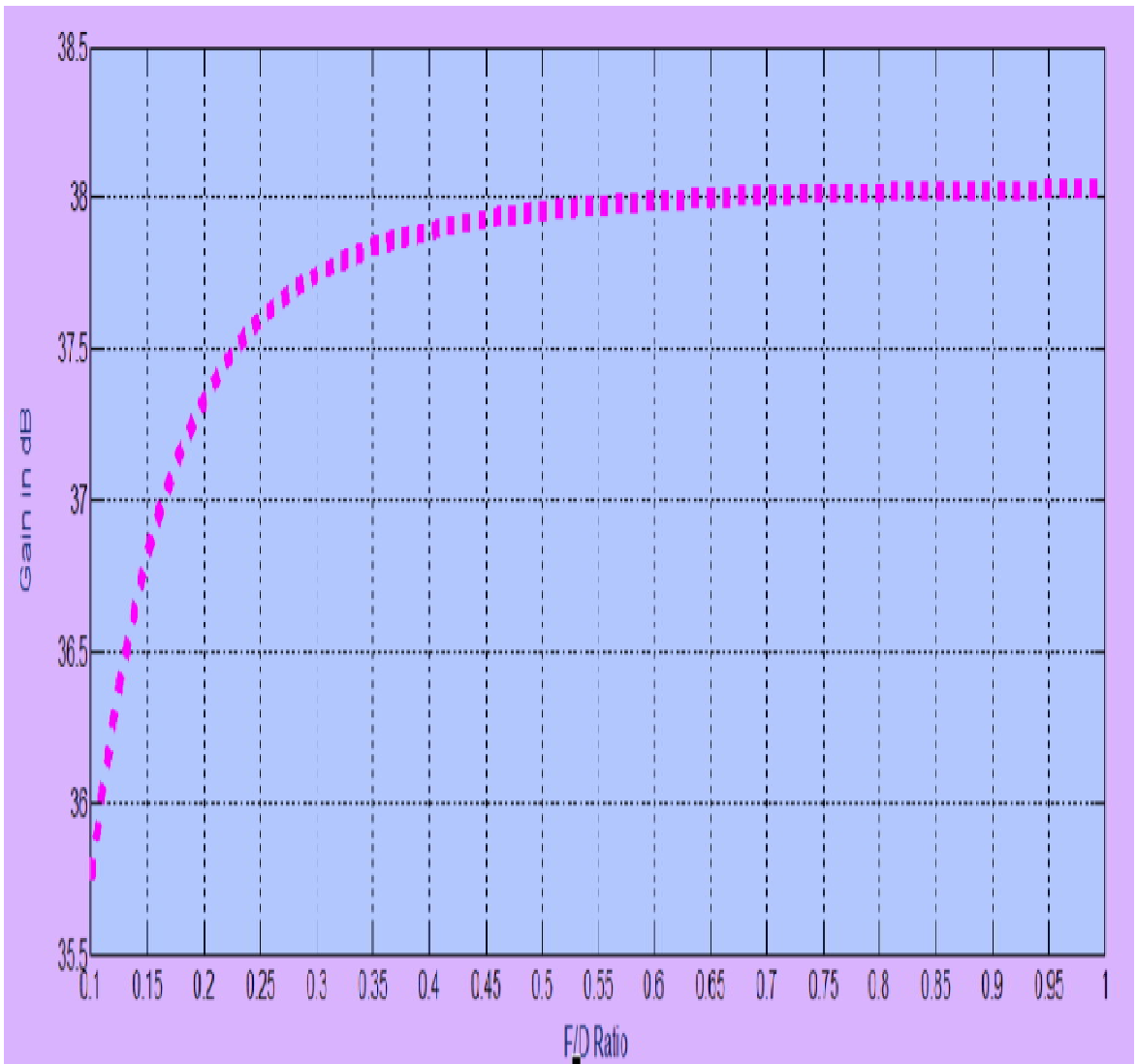


Figure (4.2) Plot of Gain as a function of F/D ratio

In figure (4.2) the response curve illustrates gain with respect to F/D ratio.

The maximum reflector antenna gain and the maximum efficiency are found by taking the most appropriate F/D ratio as shown in the above figure

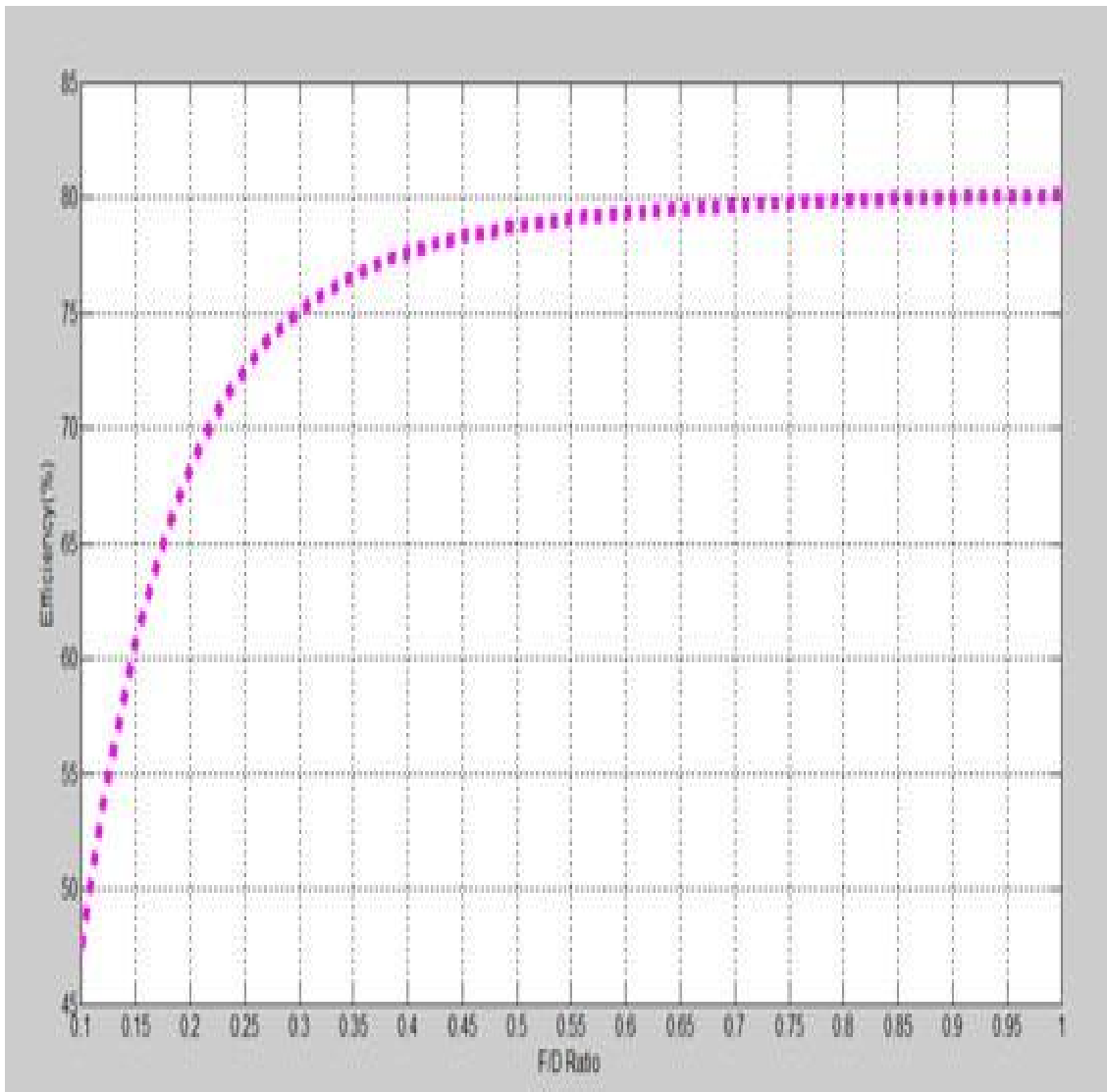


Figure (4.3) Plot of efficiency as the function of F/D

In figure (4.3) and figure (4.2) the maximum gain and efficiency is superimposed for F/D value 0.45 and then these values are constant when F/D is increase to 0.5,0.55,and so on

4.3 Helical Antenna Parameters Configuration Result

To configure and forecast the results to get optimum values, calculation and measurement for helical antenna have been done with the help of software package MATLAB.

Table (4.1) Calculation of Various Parameters of Helical Antenna

<i>Turn Spacing $N*\lambda$</i>	0.24	0.23	0.22	0.21	0.20	0.19	0.18
<i>Wavelength (mm)</i>	176.4	176.4	176.4	176.4	176.4	176.4	176.4
<i>Ideal Diameter (mm)</i>	61.3	61.3	61.3	61.3	61.3	61.3	61.3
<i>Gain (dB)</i>	14.64	14.84	15.05	15.27	15.49	15.73	15.98
<i>Conductor Diameter d (mm)</i>	3.5	3.5	3.5	3.5	3.5	3.5	3.5
<i>Winding Step (mm)</i>	42.3	40.5	38.8	37.0	35.2	33.5	31.7
<i>Adapter Separation (mm)</i>	1.7	1.7	1.7	1.7	1.7	1.7	1.7
<i>Conductor Length (mm)</i>	2764	2759	2754	2749	2745	2741	2736
<i>Reflector Diameter (mm)</i>	109.4	109.4	109.4	109.4	109.4	109.4	109.4

Table (4.1) shows that the change of helical turn spacing affects directly the helical gain. Decrease of turn spacing of helical antenna decreases the helical gain and increasing of turn spacing is decreases the gain

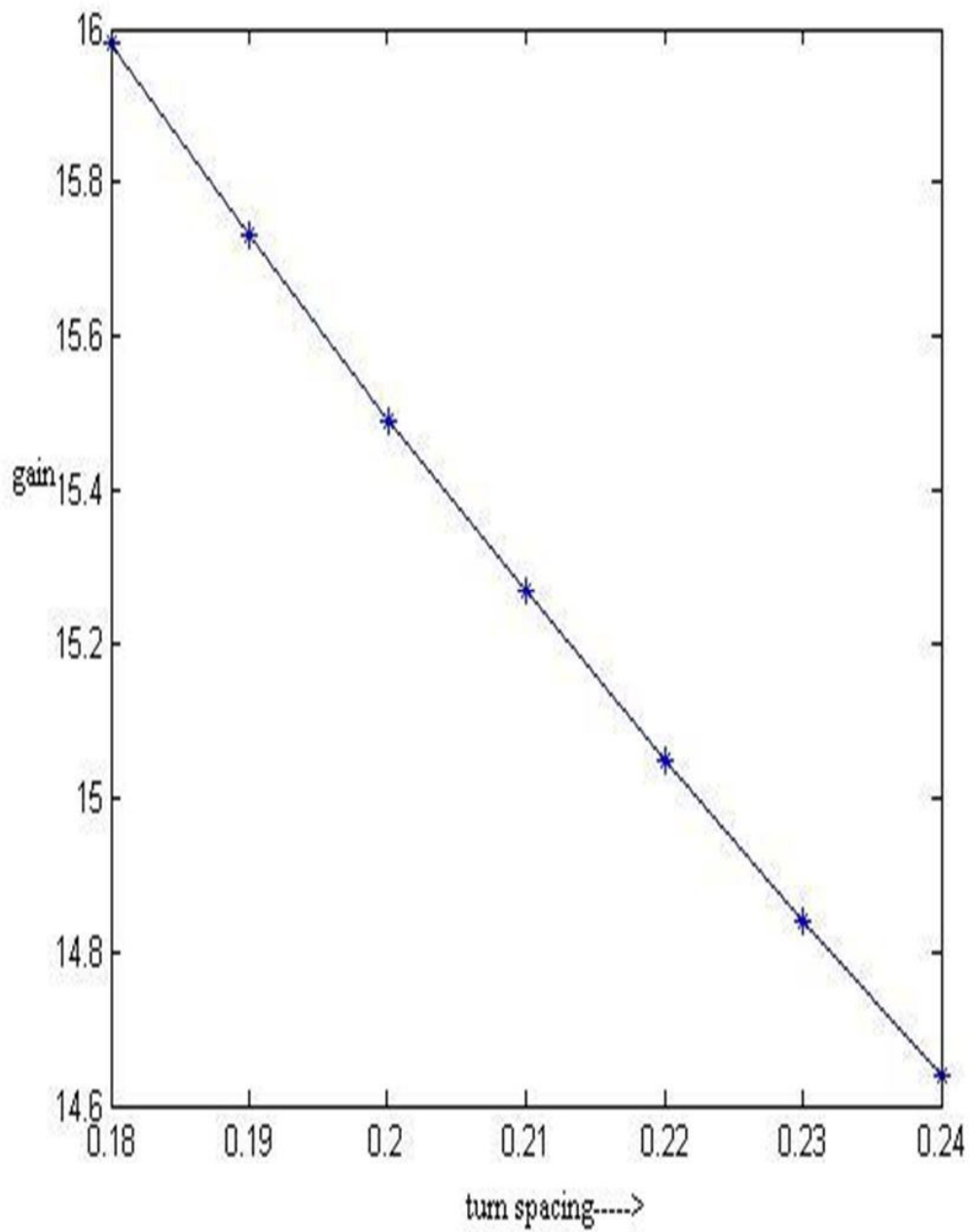


Figure (4.4) Plot of turn spacing Vs. gain

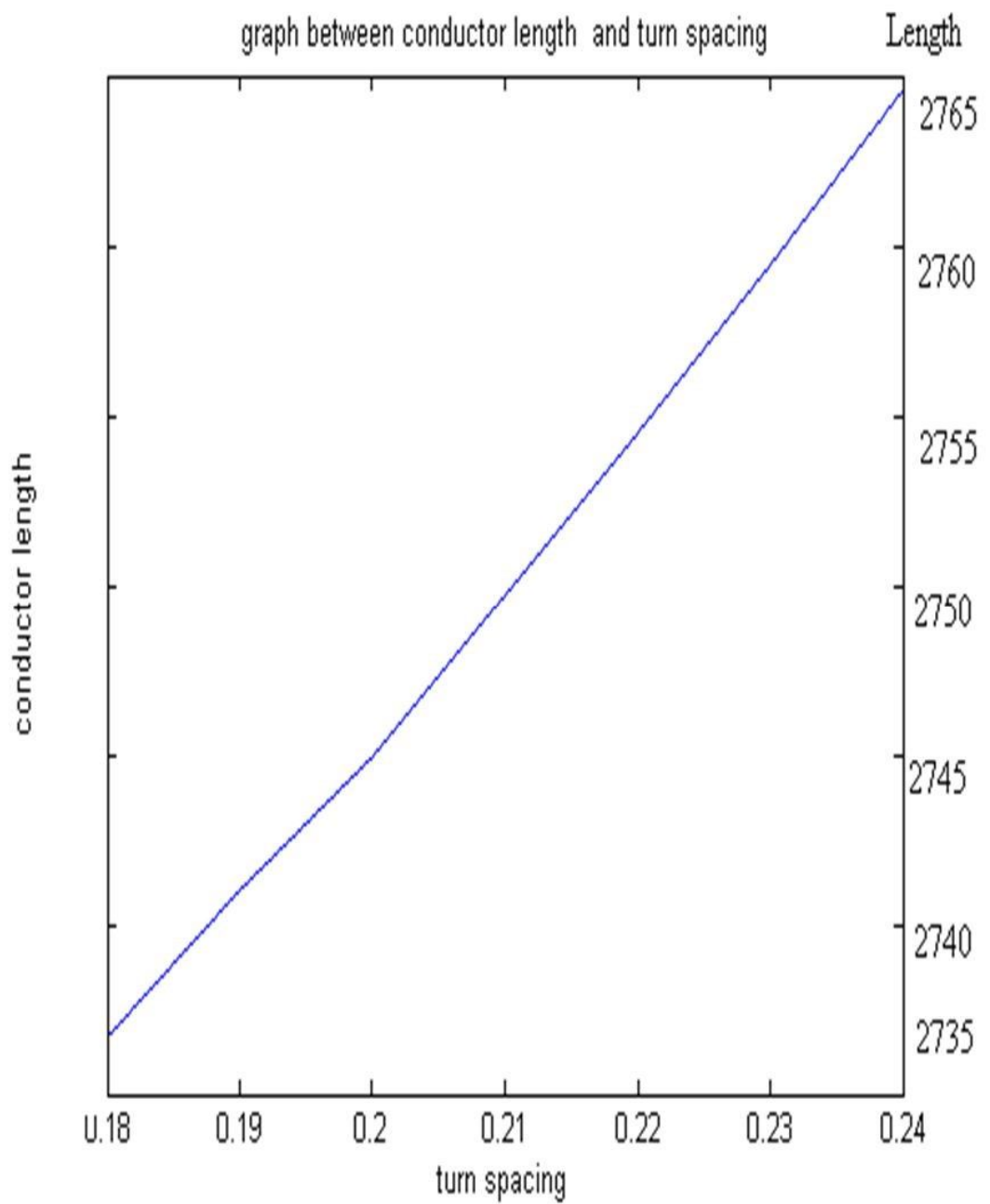


Figure (4.5) Plot of turn spacing vs. conductor length

4.4 Main Program of Research Results

Table (4.2) shows the results obtained when implementing the design and running the program. It is assumed that the initial diameter of the parabolic antenna is equal (100 Cm.) and ($\lambda = 10$ Cm.). Applying the equation, the gain equals obtained approximately 23.52 db. When the four stepper motors move one step inwards or outwards, the parabolic antenna gain increases or decreases by (10 %) respectively.

Table (4.2) results when running the program

Stepper Motors	No of Inwards Steps	No of Outwards Steps	The gain (G) In (dB)
ALL	1		23
ALL	2		22.6
ALL	3		22.1
ALL	4		21.7
ALL		1	23.9
ALL		2	24.3
ALL		3	24.7
ALL		4	25.1

Table (4.3) results when running program inward

Stepper Motors	No. of Inwards Steps	The gain (G) In (dB)
ALL	1	23
ALL	2	22.6
ALL	3	22.1
ALL	4	21.7

Table (4.3) shows the decrease of parabolic reflector gain when the diameter of dish is decrease according to inwards steps of stepper motor. The relation between minimizing the diameter and gain is illustrate at figure (4.6) below

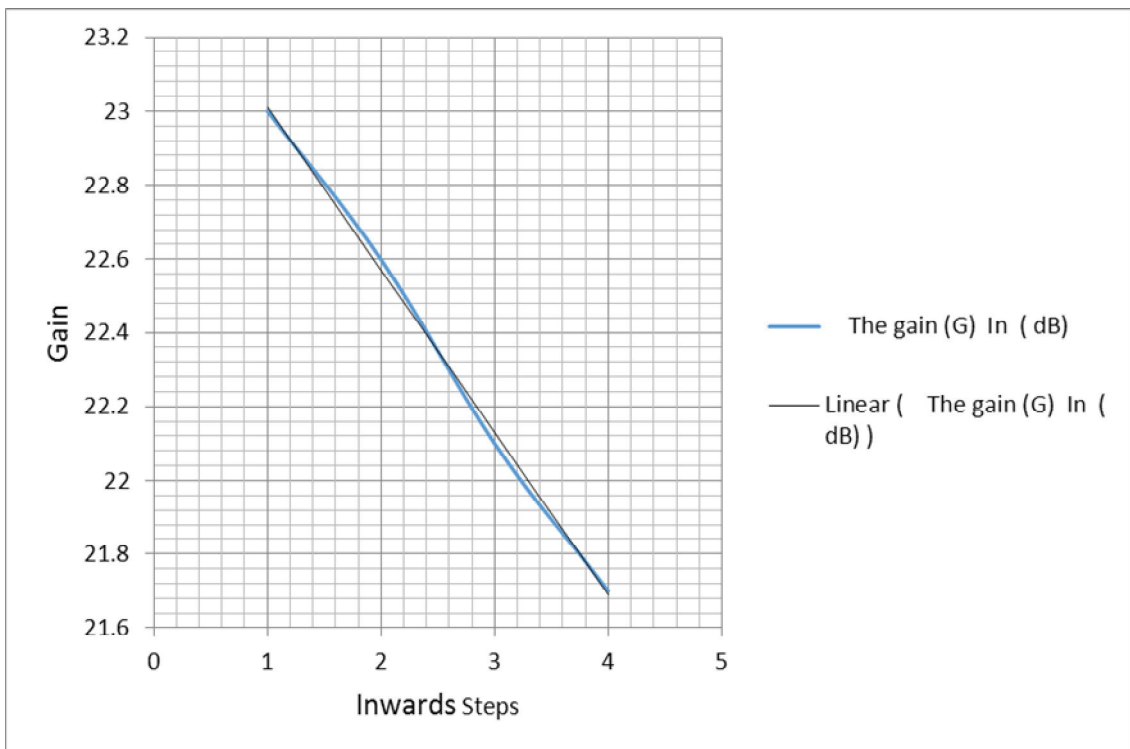


Figure (4.6) Plot of Inwards Steps Vs. Parabolic reflector Gain

Table (4.4) result when running program outwards

Stepper Motors	No. of Outwards steps	The gain (G) In (dB)
ALL	1	23.9
ALL	2	24.3
ALL	3	24.7
ALL	4	25.1

Table (4.4) shows the increasing of parabolic reflector antenna gain by the increasing of antenna diameter when the stepper motor moved outwards step. The result of increasing is also shown clearly in figure (4.7) below

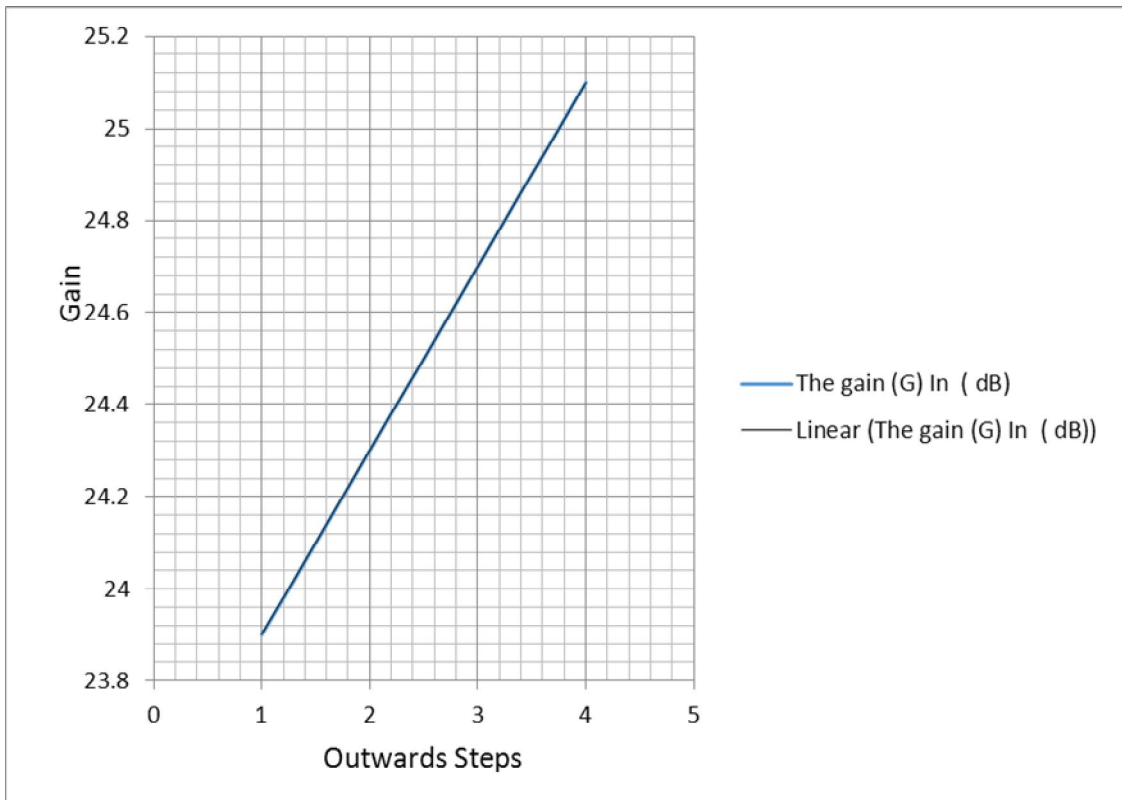


Figure (4.7) Plot of outwards Steps Vs. Parabolic reflector Gain

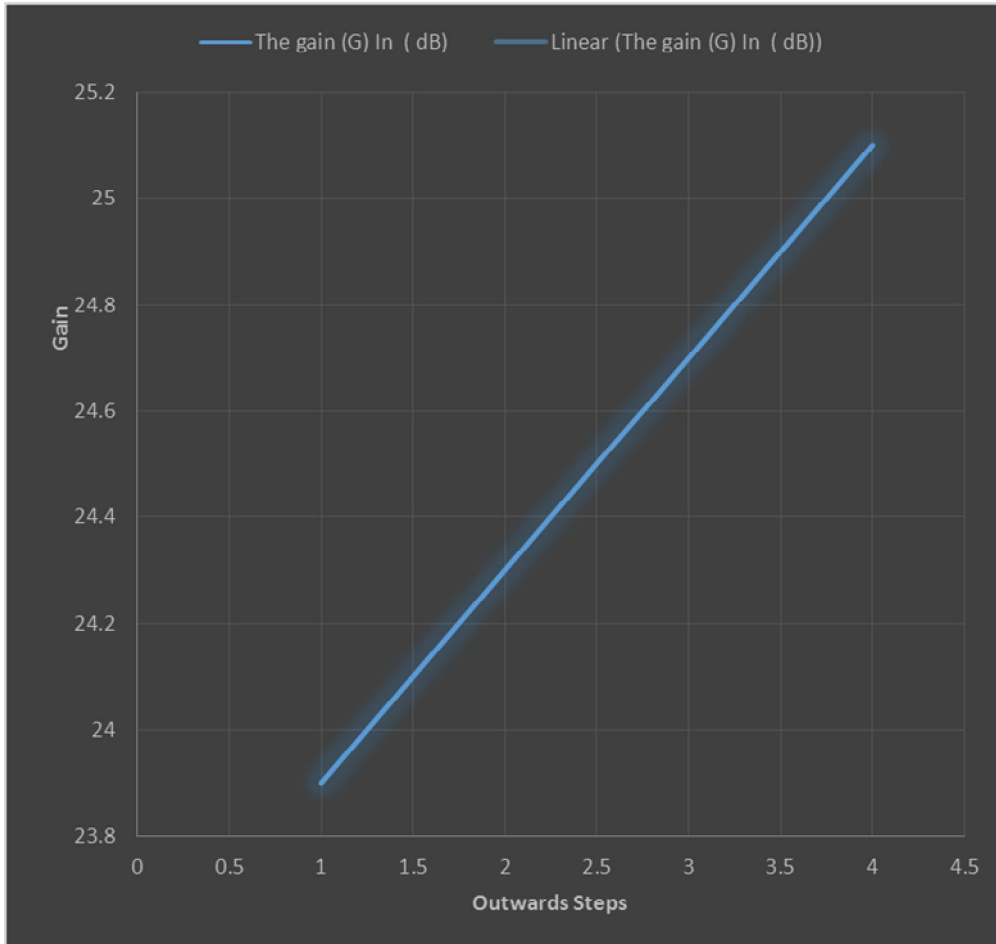


Figure (4.8) Plot of Diameter Increase Vs. Gain

Table (4.5) shows the results obtained when implementing the design and running the program. It is assumed that the initial gain of the helical antenna is equal approximately (100 or 20dB). Any step the stepper motor makes changes the gain by ($\pm 10\%$)

Table (4.5) results when running the program

No. of outwards steps	No. of inwards steps	Helical antenna gain (G) in dB
1		19.5
2		19
3		18.6
4		18.1
	1	21
	2	21.32
	3	21.5
	4	21.65

Table (4.6) results when running the program as out wards steps

No. of outwards steps	Helical antenna gain (G) in dB
1	19.5
2	19
3	18.6
4	18.1

Table (4.6) is about the relation between outwards steps which increase the helical turn spacing and the helical gain

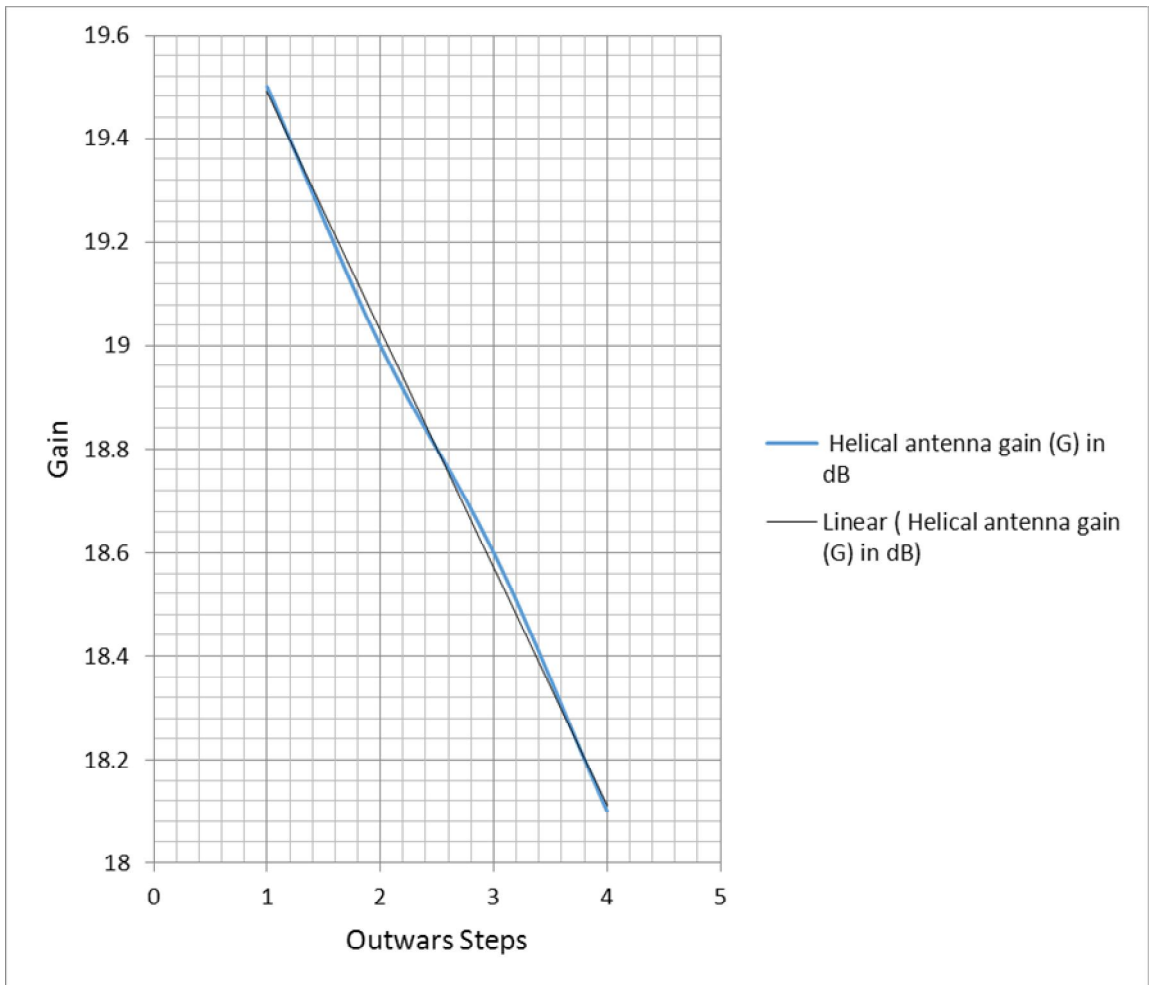


Figure (4.9) is Plot of Outwards Steps Vs. Helical Gain

Figure (4.9) shows the graph of helical gain against the outwards steps which increases the turn spacing

Table (4.7) results when running the program inwards steps

No. of inwards steps	Helical antenna gain (G) in dB
1	21
2	21.32
3	21.5
4	21.65

Table (4.7) shows the values of helical antenna gain when the turn spacing of helical antenna is decreased

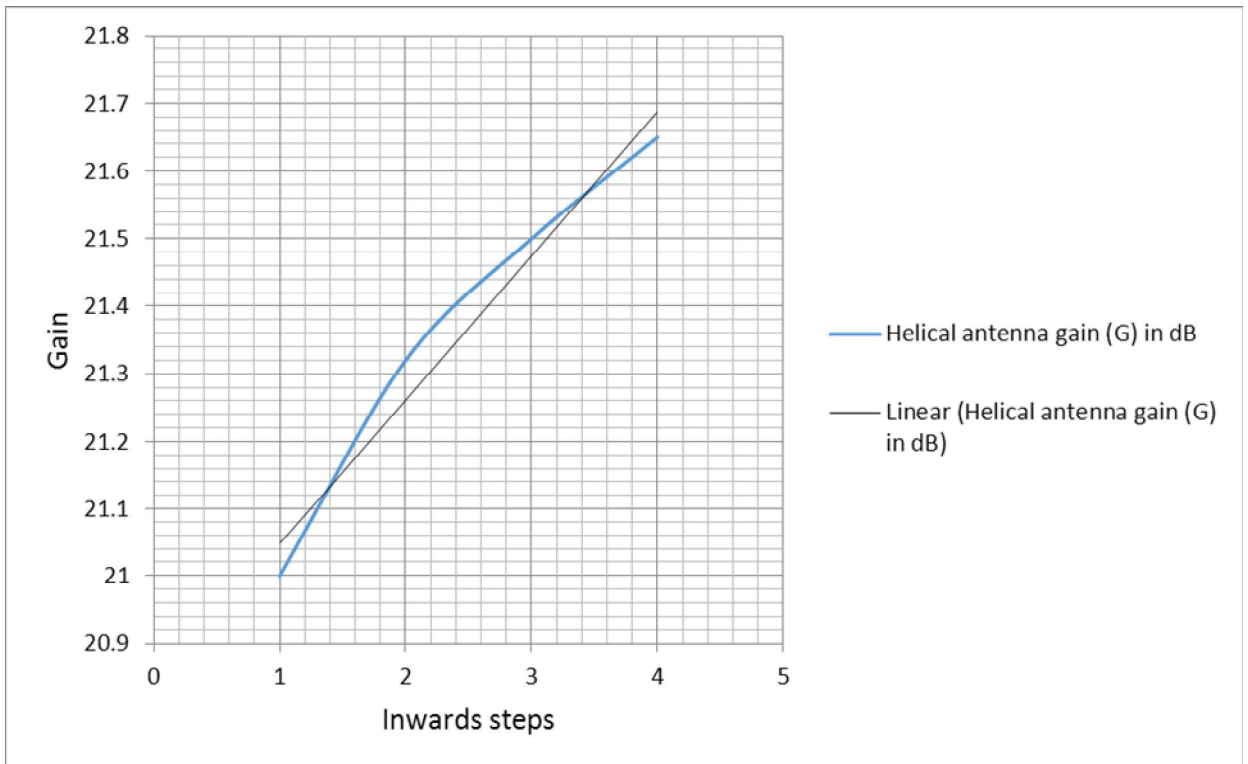


Figure (4.10) Plot of Inwards Steps Vs. Helical Gain

Figure (4.10) and figure (4.11) show the relation between helical antenna gain and turn spacing of helical antenna .The gain of antenna is increasing when the turn spacing decreases .when the turn spacing of helical antenna have been decreased the antenna conductance length also decreases and the gain is increases

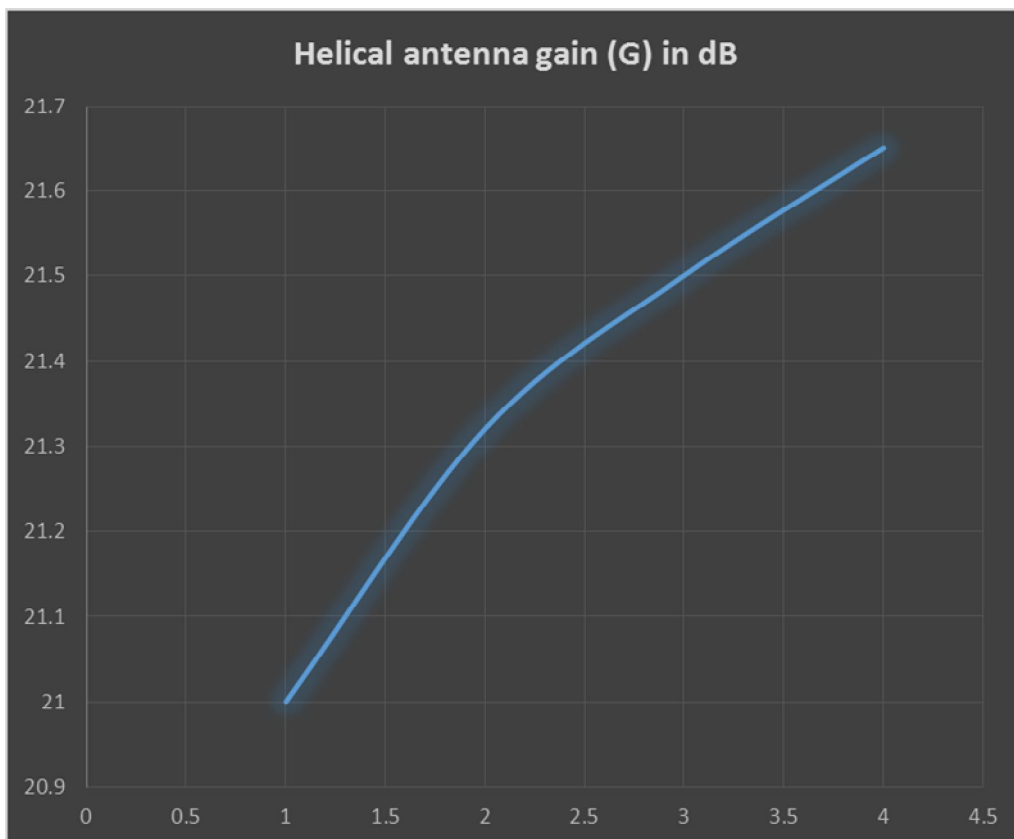


Fig (4.11) Plot of Inwards Turn Spacing Vs. Helical Gain

Chapter Five

Conclusion and Recommendation

5.1 Conclusion

The system design consists of two part of control, parabolic reflector antenna dish and the feeder of parabolic reflector antenna (helical antenna).

The structure of the parabolic antenna dish is made of four interlaced sectors .A stepper motor is mounted on each sector to control its movement inwards or outwards. Now when the four stepper motors move the dish sectors inwards or outwards, the antenna diameter gets changed. According to the change in the diameter the parabolic antenna gain will change. This means that the parabolic antenna gain is flexible and can be varied by changing its diameter.

The fifth stepper motor is mounted with mechanical gears to drive the helix outwards or inwards. This movement changes the helix diameter and hence changes the number of turns. This leads to a change of the antenna gain.

This means that the helical feed parabolic antenna gain is flexible and can be varied by manipulating the number of turns of the helix.

By this research the following procedure to control the gain of parabolic reflector antenna, the gain have been changed with two ways .Firstly when changed the dish diameter and secondly with changed the turn spacing of helical antenna .this ways gives the system optimum solution which there are two options to control the gain.

5.2 Recommendation

The Main handicap in the design is response time of the electronic circuit. Reduction of the response time of the electronic circuit makes the design better. Very fast response integrated circuits are recommended to be used in the electronic circuit.

In addition there is other version of stepper motor such as micro stepper motor which has more accuracy and sensitivity, in future it is suggested to be implemented for higher accuracy.

The microcontroller used in the research is atmega 32; however there are many types at field so as NTEL, BASIC STAMP, and PIC.in future research it is suggested to be implemented for there are many options for usage of microcontroller.

In the future work, FPGA is suggested to be implemented, also it recommend using a horn antenna as feeder to be other option regarding feeder

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Appendix

Appendix

Software Code

'Antenna Parameters control

'Engineer Zohair Elhassan

\$regfile = "m32def.dat"

' we use the M32

\$crystal = 1000000

\$baud = 9600

'LCD CONFIGURATION

'-----

Config LCD = 40 * 2

Config Lcdpin = Pin, Db4 = Portd.4, Db5 = Portd.5, Db6 = Portd.6, Db7 = Portd.7, E = Portd.3,
Rs = Portd.2

Cls

Cursor Off

'Declaration of variables (the four sectors of the dish)

Dim Sector1 As Integer

Dim Sector2 As Integer

Dim Sector3 As Integer

Dim Sector4 As Integer

'Declaration of the number of steps for (the four sectors of the dish)

Dim Numstepsd As Integer

'Declaration of the number of steps for (the helix)

Dim Numstepsh As Integer

' program PORTB as input from the keypad

Config Pinb.0 = Input ' steps counter

Config Pinb.1 = Input

Config Pinb.2 = Input

Config Pinb.3 = Input

Config Pinb.4 = Input

Config Pinb.7 = Input ' termination of steps

Sector1 = 0

Sector2 = 0

Sector3 = 0

Sector4 = 0

Lcd "START OPERATION"

Waitms 5000

Cls

Lcd "INITIALIZATION OF PORTS"

' program PORTA as output to two stepper motors of dis

Config Porta.0 = Output

Config Porta.1 = Output

Config Porta.2 = Output

Config Porta.3 = Output

Config Porta.4 = Output

Config Porta.5 = Output

Config Porta.6 = Output

Config Porta.7 = Output

' program PORTC as output to two stepper motors of dish

Config Portc.0 = Output

Config Portc.1 = Output

Config Portc.2 = Output

Config Portc.3 = Output

Config Portc.4 = Output

Config Portc.5 = Output

Config Portc.6 = Output

Config Portc.7 = Output

' program PORTD0-3 as output to one stepper motor for helix

Config Portd.0 = Output

Config Portd.1 = Output

Config Portd.2 = Output

Config Portd.3 = Output

' program PORTB4-7 as output to one stepper motor for helix

'Config Portb.4 = Output

'Config Portb.5 = Output

'Config Portb.6 = Output

'Config Portb.7 = Output

Waitms 5000

'Specify the number of steps for the dish

Do

 If Pinb.0 = 1 Then

Numstepsd = Numstepsd + 1

Cls

Lcd "NUMBER OF STEPS IS" ; Numstepsd

Waitms 1000

Else

Numstepsd = Numstepsd

End If

If Pinb.7 = 1 Then

Goto Checksector

Cls

Lcd "NUMBER OF STEPS IS" ; Numstepsd

Waitms 1000

Else

Numstepsd = Numstepsd

End If

Loop

'Check the keypad input

Check sector:

If Pinb.1 = 1 Then

Waitms 2000

```
Goto Sector90
Else
Sector1 = Sector1
End If
If Pinb.2 = 1 Then
    Waitms 2000
    Goto Sector180
Else
Sector2 = Sector2
End If
If Pinb.3 = 1 Then
    Waitms 2000
    Goto Sector270
Else
Sector3 = Sector3
End If
If Pinb.4 = 1 Then
    Waitms 2000
    Goto Sector360
Else
Sector4 = Sector4
End If
```

Sector90:

Sector180:

Sector270:

Sector360:

Do

Cls

Lcd "sector1,2,3,4 movement" ; Numstepsd

 Waitms 1000

'move one step sector1

 Porta.0 = 1

 Porta.1 = 0

 Porta.2 = 0

 Porta.3 = 0

'move one step sector2

 Porta.4 = 1

 Porta.5 = 0

 Porta.6 = 0

 Porta.7 = 0

'move one step sector3

Portc.0 = 1

Portc.1 = 0

Portc.2 = 0

Portc.3 = 0

'move one step sector4

Portc.4 = 1

Portc.5 = 0

Portc.6 = 0

Portc.7 = 0

'decrement numsteps

Numstepsd = Numstepsd - 1

If Numstepsd = 0 Then

 Waitms 2000

 Goto Finishstepsd

Else

 Numstepsd = Numstepsd

End If

Cls

Lcd "sector1,2,3,4 movement" ; Numstepsd

Waitms 1000

'move one step sector1

Porta.0 = 0

Porta.1 = 1

Porta.2 = 0

Porta.3 = 0

'move one step sector2

Porta.4 = 0

Porta.5 = 1

Porta.6 = 0

Porta.7 = 0

'move one step sector3

Portc.0 = 0

Portc.1 = 1

Portc.2 = 0

Portc.3 = 0

'move one step sector4

Portc.4 = 0

Portc.5 = 1

Portc.6 = 0

Portc.7 = 0

'decrement numsteps

Numstepsd = Numstepsd - 1

If Numstepsd = 0 Then

Waitms 2000

Goto Finishstepsd

Else

Numstepsd = Numstepsd

End If

Cls

Lcd "sector1,2,3,4 movement" ; Numstepsd

Waitms 1000

'move one step sector1

Porta.0 = 0

Porta.1 = 0

Porta.2 = 1

Porta.3 = 0

'move one step sector2

Porta.4 = 0

Porta.5 = 0

Porta.6 = 1

Porta.7 = 0

'move one step sector3

Portc.0 = 0

Portc.1 = 0

Portc.2 = 1

Portc.3 = 0

'move one step sector4

Portc.4 = 0

Portc.5 = 0

Portc.6 = 1

Portc.7 = 0

'decrement numsteps

Numstepsd = Numstepsd - 1

If Numstepsd = 0 Then

 Waitms 2000

 Goto Finishstepsd

Else

Numstepsd = Numstepsd

End If

Cls

Lcd "sector1,2,3,4 movement" ; Numstepsd

Waitms 1000

'move one step sector1

Porta.0 = 0

Porta.1 = 0

Porta.2 = 0

Porta.3 = 1

'Move one step sector2

Porta.4 = 0

Porta.5 = 0

Porta.6 = 0

Porta.7 = 1

'move one step sector3

Portc.0 = 0

Portc.1 = 0

Portc.2 = 0

Portc.3 = 1

'move one step sector4

Portc.4 = 0

Portc.5 = 0

Portc.6 = 0

Portc.7 = 1

'decrement numsteps

Numstepsd = Numstepsd - 1

If Numstepsd = 0 Then

 Waitms 2000

 Goto Finishstepsd

Else

 Numstepsd = Numstepsd

End If

Loop

Finishstepsd:

Cls

Lcd "DISH IS POSITIONED" ; Numstepsd

Waitms 1000

'Helix movement

'Specify the number of steps for the helix

Do

If Pinb.0 = 1 Then

Numstepsh = Numstepsh + 1

Cls

Lcd "NUMBER OF STEPS FOR HELIX IS" ; Numstepsh

Waitms 1000

Else

Numstepsh = Numstepsh

End If

If Pinb.7 = 1 Then

Goto Helixturns

Cls

Lcd "NUMBER OF STEPS FOR HELIX IS" ; Numstepsh

Waitms 1000

Else

```
    Numstepsh = Numstepsh
End If
Loop

Helixturns:

Do
Cls
Lcd "HELIX movement" ; Numstepsh
    Waitms 1000
'move helix one step
    Portd.0 = 1
    Portd.1 = 0
    Portd.2 = 0
    Portd.3 = 0

'decrement numstepsh
    Numstepsh = Numstepsh - 1

If Numstepsh = 0 Then
    Waitms 2000
    Goto Finishstepsh
```


Else

Numstepsh = Numstepsh

End If

Cls

Lcd "HELIX movement" ; Numstepsh

Waitms 1000

'move helix one step

Portd.0 = 0

Portd.1 = 1

Portd.2 = 0

Portd.3 = 0

'decrement numstepsh

Numstepsh = Numstepsh - 1

If Numstepsh = 0 Then

Waitms 2000

Goto Finishstepsh

Else

Numstepsh = Numstepsh

End If

```
Cls
Lcd "HELIX movement" ; Numstepsh
  Waitms 1000
'move helix one step
  Portd.0 = 0
  Portd.1 = 0
  Portd.2 = 1
  Portd.3 = 0
```

```
'decrement numstepsh
  Numstepsh = Numstepsh - 1
```

```
If Numstepsh = 0 Then
  Waitms 2000
  Goto Finishstepsh
Else
  Numstepsh = Numstepsh
End If
```

```
Cls
Lcd "HELIX movement" ; Numstepsh
  Waitms 1000
```

'move helix one step

Portd.0 = 0

Portd.1 = 0

Portd.2 = 0

Portd.3 = 1

'decrement numstepsh

Numstepsh = Numstepsh - 1

If Numstepsh = 0 Then

 Waitms 2000

 Goto Finishstepsh

Else

 Numstepsh = Numstepsh

End If

Loop

Finishstepsh:

Cls

Lcd "HELIX IS POSITIONED" ; Numstepsd

Waitms 1000

End

Features

- High-performance, Low-power Atmel® AVR® 8-bit Microcontroller • Advanced RISC Architecture
 - 131 Powerful Instructions – Most Single-clock Cycle Execution
 - 32 x 8 General Purpose Working Registers
 - Fully Static Operation
 - Up to 16 MIPS Throughput at 16 MHz
 - On-chip 2-cycle Multiplier
- High Endurance Non-volatile Memory segments
 - 32Kbytes of In-System Self-programmable Flash program memory
 - 1024Bytes EEPROM
 - 2Kbyte Internal SRAM
 - Write/Erase Cycles: 10,000 Flash/100,000 EEPROM
 - Data retention: 20 years at 85°C/100 years at 25°C⁽¹⁾
 - Optional Boot Code Section with Independent Lock Bits In-System Programming by On-chip Boot Program
- True Read-While-Write Operation
 - Programming Lock for Software Security
- JTAG (IEEE std. 1149.1 Compliant) Interface
 - Boundary-scan Capabilities According to the JTAG Standard
 - Extensive On-chip Debug Support
 - Programming of Flash, EEPROM, Fuses, and Lock Bits through the JTAG Interface
- Peripheral Features
 - Two 8-bit Timer/Counters with Separate Prescalers and Compare Modes
 - One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture Mode
 - Real Time Counter with Separate Oscillator
 - Four PWM Channels
 - 8-channel, 10-bit ADC
- 8 Single-ended Channels
- 7 Differential Channels in TQFP Package Only
- 2 Differential Channels with Programmable Gain at 1x, 10x, or 200x
 - Byte-oriented Two-wire Serial Interface
 - Programmable Serial USART
 - Master/Slave SPI Serial Interface
 - Programmable Watchdog Timer with Separate On-chip Oscillator
 - On-chip Analog Comparator
- Special Microcontroller Features
 - Power-on Reset and Programmable Brown-out Detection
 - Internal Calibrated RC Oscillator
 - External and Internal Interrupt Sources
 - Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby and Extended Standby
- I/O and Packages



**8-bit AVR®
Microcontroller
with 32KBytes
In-System
Programmable
Flash**

**ATmega32
ATmega32L**

Summary

- 32 Programmable I/O Lines
- 40-pin PDIP, 44-lead TQFP, and 44-pad QFN/MLF
- Operating Voltages
 - 2.7V - 5.5V for ATmega32L
 - 4.5V - 5.5V for ATmega32
- Speed Grades
 - 0 - 8MHz for ATmega32L
 - 0 - 16MHz for ATmega32
- Power Consumption at 1 MHz, 3V, 25°C
 - Active: 1.1mA
 - Idle Mode: 0.35mA
 - Power-down Mode: < 1µA

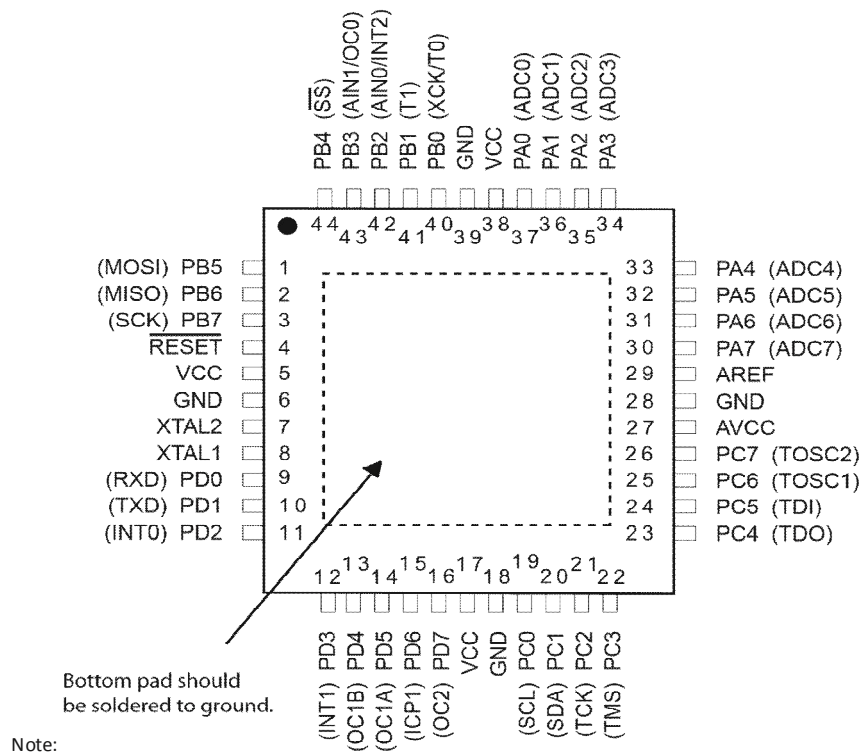
Pin Configurations

Figure 1. Pinout ATmega32

(XCK/T0) PB0	1	40	PA0 (ADC0)
(T1) PB1	2	39	PA1 (ADC1)
(INT2/AIN0) PB2	3	38	PA2 (ADC2)
(OC0/AIN1) PB3	4	37	PA3 (ADC3)
(SS) PB4	5	36	PA4 (ADC4)
(MOSI) PB5	6	35	PA5 (ADC5)
(MISO) PB6	7	34	PA6 (ADC6)
(SCK) PB7	8	33	PA7 (ADC7)
RESET	9	32	AREF
VCC	10	31	GND
GND	11	30	AVCC
XTAL2	12	29	PC7 (TOSC2)
XTAL1	13	28	PC6 (TOSC1)
(RXD) PD0	14	27	PC5 (TDI)
(TXD) PD1	15	26	PC4 (TDO)
(INT0) PD2	16	25	PC3 (TMS)
(INT1) PD3	17	24	PC2 (TCK)
(OC1B) PD4	18	23	PC1 (SDA)
(OC1A) PD5	19	22	PC0 (SCL)
(ICP1) PD6	20	21	PD7 (OC2)

PDIP

TQFP/MLF

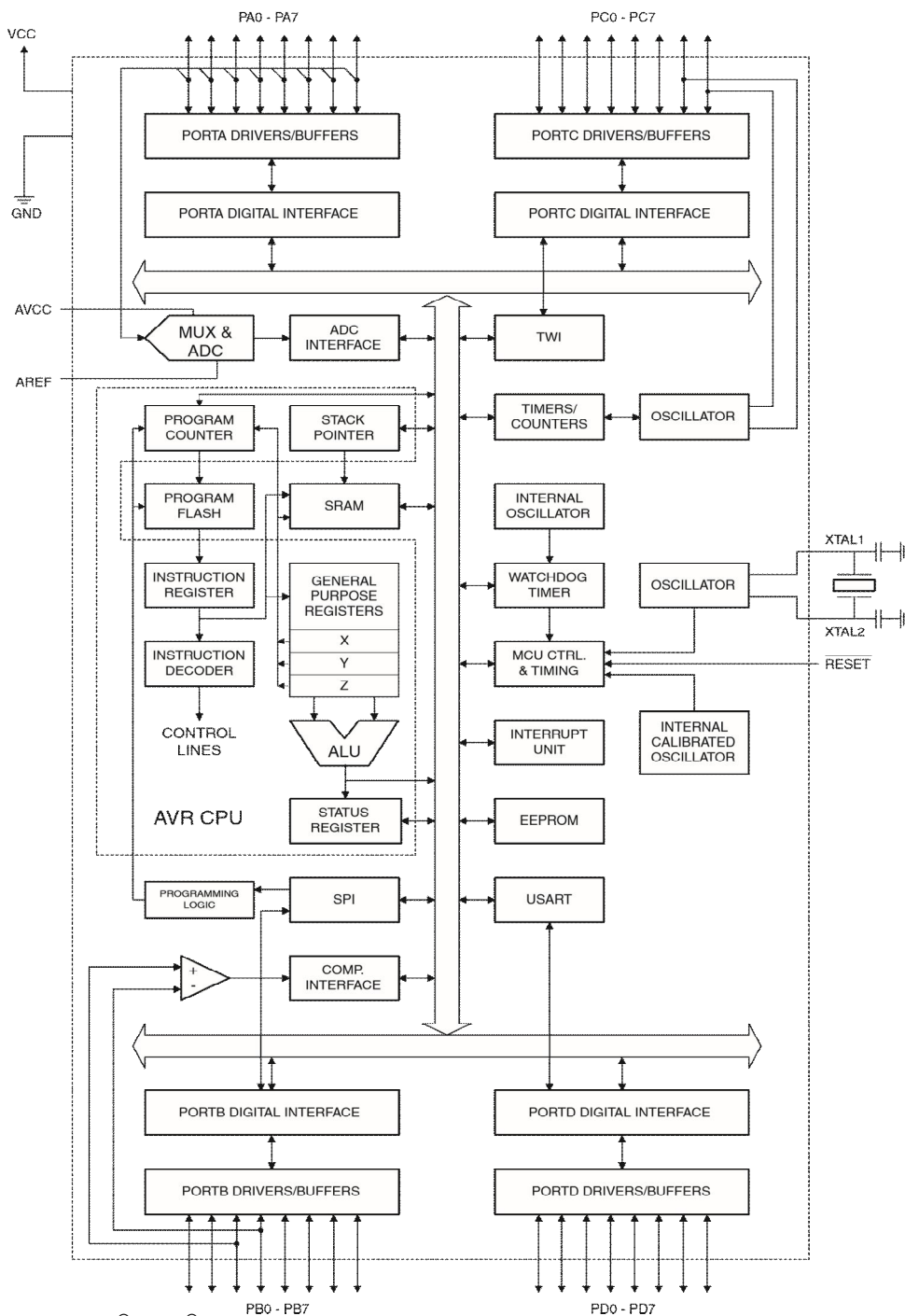


Overview

The Atmel® AVR® ATmega32 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega32 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

Block Diagram

Figure 2. Block Diagram



The Atmel® AVR® core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATmega32 provides the following features: 32Kbytes of In-System Programmable Flash Program memory with Read-While-Write capabilities, 1024bytes EEPROM, 2Kbyte SRAM, 32 general purpose I/O lines, 32 general purpose working registers, a JTAG interface for Boundary scan, On-chip Debugging support and programming, three flexible Timer/Counters with compare modes, Internal and External Interrupts, a serial programmable USART, a byte oriented

Two-wire Serial Interface, an 8-channel, 10-bit ADC with optional differential input stage with programmable gain (TQFP package only), a programmable Watchdog Timer with Internal Oscillator, an SPI serial port, and six software selectable power saving modes. The Idle mode stops the CPU while allowing the USART, Two-wire interface, A/D Converter, SRAM, Timer/Counters, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next External Interrupt or Hardware Reset. In Power-save mode, the Asynchronous Timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except Asynchronous Timer and ADC, to minimize switching noise during ADC conversions. In Standby mode, the crystal/resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low-power consumption. In Extended Standby mode, both the main Oscillator and the Asynchronous Timer continue to run.

The device is manufactured using Atmel's high density nonvolatile memory technology. The Onchip ISP Flash allows the program memory to be reprogrammed in-system through an SPI serial interface, by a conventional nonvolatile memory programmer, or by an On-chip Boot program running on the AVR core. The boot program can use any interface to download the application program in the Application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATmega32 is a powerful microcontroller that provides a highly-flexible and cost-effective solution to many embedded control applications.

The Atmel AVR ATmega32 is supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, in-circuit emulators, and evaluation kits.

Pin Descriptions

VCC Digital supply voltage.

GND Ground.

Port A (PA7..PA0) Port A serves as the analog inputs to the A/D Converter.

Port A also serves as an 8-bit bi-directional I/O port, if the A/D Converter is not used. Port pins can provide internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability. When pins PA0 to PA7 are used as inputs and are externally pulled low, they will source current if the internal pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B (PB7..PB0) Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B also serves the functions of various special features of the ATmega32 as listed on [page 57](#).

Port C (PC7..PC0)

Port C is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running. If the JTAG interface is enabled, the pull-up resistors on pins PC5(TDI), PC3(TMS) and PC2(TCK) will be activated even if a reset occurs.

The TD0 pin is tri-stated unless TAP states that shift out data are entered.

Port C also serves the functions of the JTAG interface and other special features of the ATmega32 as listed on [page 60](#).

Port D (PD7..PD0)

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port D also serves the functions of various special features of the ATmega32 as listed on [page 62](#).

RESET

Reset Input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in [Table 15 on page 37](#). Shorter pulses are not guaranteed to generate a reset.

XTAL1

Input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting Oscillator amplifier.

AVCC

AVCC is the supply voltage pin for Port A and the A/D Converter. It should be externally connected to V_{CC} , even if the ADC is not used. If the ADC is used, it should be connected to V_{CC} through a low-pass filter.

AREF

AREF is the analog reference pin for the A/D Converter.

Resources

A comprehensive set of development tools, application notes and datasheets are available for download on <http://www.atmel.com/avr>.

Data Retention

Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.

About Code Examples

This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C Compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C Compiler documentation for more details.

Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
\$3F (\$5F)	SREG	I	T	H	S	V	N	Z	C	10
\$3E (\$5E)	SPH	–	–	–	–	SP11	SP10	SP9	SP8	12
\$3D (\$5D)	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	12
\$3C (\$5C)	OCR0	Timer/Counter0 Output Compare Register								82
\$3B (\$5B)	GICR	INT1	INT0	INT2	–	–	–	IVSEL	IVCE	47, 67
\$3A (\$5A)	GIFR	INTF1	INTF0	INTF2	–	–	–	–	–	68
\$39 (\$59)	TIMSK	OCIE2	TOIE2	TICIE1	OCIE1A	OCIE1B	TOIE1	OCIE0	TOIE0	82, 112, 130
\$38 (\$58)	TIFR	OCF2	TOV2	ICF1	OCF1A	OCF1B	TOV1	OCF0	TOV0	83, 112, 130
\$37 (\$57)	SPMCR	SPMIE	RWWSB	–	RWWSRE	BLBSET	PGWRT	PGERS	SPMEN	248
\$36 (\$56)	TWCR	TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	–	TWIE	177
\$35 (\$55)	MCUCR	SE	SM2	SM1	SM0	ISC11	ISC10	ISC01	ISC00	32, 66
\$34 (\$54)	MCUCSR	JTD	ISC2	–	JTRF	WDRF	BORF	EXTRF	PORF	40, 67, 228
\$33 (\$53)	TCCR0	FOC0	WGM00	COM01	COM00	WGM01	CS02	CS01	CS00	80
\$32 (\$52)	TCNT0	Timer/Counter0 (8 Bits)								82
\$31(n) (\$51)(n)	OSCCAL	Oscillator Calibration Register								30
	OCDR	On-Chip Debug Register								224
\$30 (\$50)	SFIOR	ADTS2	ADTS1	ADTS0	–	ACME	PUD	PSR2	PSR10	56,85,131,198,218
\$2F (\$4F)	TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	FOC1A	FOC1B	WGM11	WGM10	107
\$2E (\$4E)	TCCR1B	ICNC1	ICES1	–	WGM13	WGM12	CS12	CS11	CS10	110
\$2D (\$4D)	TCNT1H	Timer/Counter1 – Counter Register High Byte								111
\$2C (\$4C)	TCNT1L	Timer/Counter1 – Counter Register Low Byte								111
\$2B (\$4B)	OCR1AH	Timer/Counter1 – Output Compare Register A High Byte								111
\$2A (\$4A)	OCR1AL	Timer/Counter1 – Output Compare Register A Low Byte								111
\$29 (\$49)	OCR1BH	Timer/Counter1 – Output Compare Register B High Byte								111
\$28 (\$48)	OCR1BL	Timer/Counter1 – Output Compare Register B Low Byte								111
\$27 (\$47)	ICR1H	Timer/Counter1 – Input Capture Register High Byte								111
\$26 (\$46)	ICR1L	Timer/Counter1 – Input Capture Register Low Byte								111
\$25 (\$45)	TCCR2	FOC2	WGM20	COM21	COM20	WGM21	CS22	CS21	CS20	125
\$24 (\$44)	TCNT2	Timer/Counter2 (8 Bits)								127
\$23 (\$43)	OCR2	Timer/Counter2 Output Compare Register								127
\$22 (\$42)	ASSR	–	–	–	–	AS2	TCN2UB	OCR2UB	TCR2UB	128
\$21 (\$41)	WDTCR	–	–	–	WDTOE	WDE	WDP2	WDP1	WDP0	42
\$20(z) (\$40)(z)	UBRRH	URSEL	–	–	–	UBRR[11:8]				164
	UCSRC	URSEL	UMSEL	UPM1	UPM0	USBS	UCSZ1	UCSZ0	UCPOL	162
\$1F (\$3F)	EEARH	–	–	–	–	–	–	EEAR9	EEAR8	19
\$1E (\$3E)	EEARL	EEPROM Address Register Low Byte								19
\$1D (\$3D)	EEDR	EEPROM Data Register								19
\$1C (\$3C)	EEDR	–	–	–	–	EERIE	EEMWE	EEWE	EERE	19
\$1B (\$3B)	PORTA	PORTA7	PORTA6	PORTA5	PORTA4	PORTA3	PORTA2	PORTA1	PORTA0	64
\$1A (\$3A)	DDRA	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	64
\$19 (\$39)	PINA	PINA7	PINA6	PINA5	PINA4	PINA3	PINA2	PINA1	PINA0	64

\$18 (\$38)	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	64
\$17 (\$37)	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	64
\$16 (\$36)	PINB	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	65
\$15 (\$35)	PORTC	PORTC7	PORTC6	PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0	65
\$14 (\$34)	DDRC	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	65
\$13 (\$33)	PINC	PINC7	PINC6	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0	65
\$12 (\$32)	PORTD	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	65
\$11 (\$31)	DDRD	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	65
\$10 (\$30)	PIND	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	65
\$0F (\$2F)	SPDR	SPI Data Register								138
\$0E (\$2E)	SPSR	SPIF	WCOL	–	–	–	–	–	SPI2X	138
\$0D (\$2D)	SPCR	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	136
\$0C (\$2C)	UDR	USART I/O Data Register								159
\$0B (\$2B)	UCSRA	RXC	TXC	UDRE	FE	DOR	PE	U2X	MPCM	160
\$0A (\$2A)	UCSRB	RXCIE	TXCIE	UDRIE	RXEN	TXEN	UCSZ2	RXB8	TXB8	161
\$09 (\$29)	UBRRL	USART Baud Rate Register Low Byte								164
\$08 (\$28)	ACSR	ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	199
\$07 (\$27)	ADMUX	REFS1	REFS0	ADLAR	MUX4	MUX3	MUX2	MUX1	MUX0	214
\$06 (\$26)	ADCSRA	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0	216
\$05 (\$25)	ADCH	ADC Data Register High Byte								217
\$04 (\$24)	ADCL	ADC Data Register Low Byte								217
\$03 (\$23)	TWDR	Two-wire Serial Interface Data Register								179
\$02 (\$22)	TWAR	TWA6	TWA5	TWA4	TWA3	TWA2	TWA1	TWA0	TWGCE	179
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
\$01 (\$21)	TWSR	TWS7	TWS6	TWS5	TWS4	TWS3	–	TWPS1	TWPS0	178
\$00 (\$20)	TWBR	Two-wire Serial Interface Bit Rate Register								177

Notes: 1. When the OCDEN Fuse is unprogrammed, the OSCCAL Register is always accessed on this address. Refer to the debugger specific documentation for details on how to use the OCDR Register.

2. Refer to the USART description for details on how to access UBRRH and UCSRC.
3. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
4. Some of the Status Flags are cleared by writing a logical one to them. Note that the CBI and SBI instructions will operate on all bits in the I/O Register, writing a one back into any flag read as set, thus clearing the flag. The CBI and SBI instructions work with registers \$00 to \$1F only.

Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ARITHMETIC AND LOGIC INSTRUCTIONS					
ADD	Rd, Rr	Add two Registers	$Rd \leftarrow Rd + Rr$	Z,C,N,V,H	1
ADC	Rd, Rr	Add with Carry two Registers	$Rd \leftarrow Rd + Rr + C$	Z,C,N,V,H	1
ADIW	RdI,K	Add Immediate to Word	$Rdh:Rdl \leftarrow Rdh:Rdl + K$	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract two Registers	$Rd \leftarrow Rd - Rr$	Z,C,N,V,H	1
SUBI	Rd, K	Subtract Constant from Register	$Rd \leftarrow Rd - K$	Z,C,N,V,H	1
SBC	Rd, Rr	Subtract with Carry two Registers	$Rd \leftarrow Rd - Rr - C$	Z,C,N,V,H	1
SBCI	Rd, K	Subtract with Carry Constant from Reg.	$Rd \leftarrow Rd - K - C$	Z,C,N,V,H	1
SBIW	RdI,K	Subtract Immediate from Word	$Rdh:Rdl \leftarrow Rdh:Rdl - K$	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND Registers	$Rd \leftarrow Rd \cdot Rr$	Z,N,V	1
ANDI	Rd, K	Logical AND Register and Constant	$Rd \leftarrow Rd \cdot K$	Z,N,V	1
OR	Rd, Rr	Logical OR Registers	$Rd \leftarrow Rd \vee Rr$	Z,N,V	1
ORI	Rd, K	Logical OR Register and Constant	$Rd \leftarrow Rd \vee K$	Z,N,V	1
EOR	Rd, Rr	Exclusive OR Registers	$Rd \leftarrow Rd \oplus Rr$	Z,N,V	1
COM	Rd	One's Complement	$Rd \leftarrow \$FF - Rd$	Z,C,N,V	1
NEG	Rd	Two's Complement	$Rd \leftarrow \$00 - Rd$	Z,C,N,V,H	1
SBR	Rd,K	Set Bit(s) in Register	$Rd \leftarrow Rd \vee K$	Z,N,V	1
CBR	Rd,K	Clear Bit(s) in Register	$Rd \leftarrow Rd \cdot (\$FF - K)$	Z,N,V	1
INC	Rd	Increment	$Rd \leftarrow Rd + 1$	Z,N,V	1
DEC	Rd	Decrement	$Rd \leftarrow Rd - 1$	Z,N,V	1
TST	Rd	Test for Zero or Minus	$Rd \leftarrow Rd \cdot Rd$	Z,N,V	1
CLR	Rd	Clear Register	$Rd \leftarrow Rd \oplus Rd$	Z,N,V	1
SER	Rd	Set Register	$Rd \leftarrow \$FF$	None	1
MUL	Rd, Rr	Multiply Unsigned	$R1:R0 \leftarrow Rd \times Rr$	Z,C	2
MULS	Rd, Rr	Multiply Signed	$R1:R0 \leftarrow Rd \times Rr$	Z,C	2
MULSU	Rd, Rr	Multiply Signed with Unsigned	$R1:R0 \leftarrow Rd \times Rr$	Z,C	2
FMUL	Rd, Rr	Fractional Multiply Unsigned	$R1:R0 \leftarrow (Rd \times Rr) \ll 1$	Z,C	2
FMULS	Rd, Rr	Fractional Multiply Signed	$R1:R0 \leftarrow (Rd \times Rr) \ll 1$	Z,C	2
FMULSU	Rd, Rr	Fractional Multiply Signed with Unsigned	$R1:R0 \leftarrow (Rd \times Rr) \ll 1$	Z,C	2
BRANCH INSTRUCTIONS					
RJMP	k	Relative Jump	$PC \leftarrow PC + k + 1$	None	2
IJMP		Indirect Jump to (Z)	$PC \leftarrow Z$	None	2
JMP	k	Direct Jump	$PC \leftarrow k$	None	3
RCALL	k	Relative Subroutine Call	$PC \leftarrow PC + k + 1$	None	3
ICALL		Indirect Call to (Z)	$PC \leftarrow Z$	None	3
CALL	k	Direct Subroutine Call	$PC \leftarrow k$	None	4
RET		Subroutine Return	$PC \leftarrow Stack$	None	4
RETI		Interrupt Return	$PC \leftarrow Stack$	I	4
CPSE	Rd,Rr	Compare, Skip if Equal	if $(Rd = Rr)$ $PC \leftarrow PC + 2$ or 3	None	1 / 2 / 3
CP	Rd,Rr	Compare	$Rd - Rr$	Z, N,V,C,H	1
CPC	Rd,Rr	Compare with Carry	$Rd - Rr - C$	Z, N,V,C,H	1
CPI	Rd,K	Compare Register with Immediate	$Rd - K$	Z, N,V,C,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if $(Rr(b)=0)$ $PC \leftarrow PC + 2$ or 3	None	1 / 2 / 3

SBRS	Rr, b	Skip if Bit in Register is Set	if (Rr(b)=1) PC ← PC + 2 or 3	None	1 / 2 / 3
SBIC	P, b	Skip if Bit in I/O Register Cleared	if (P(b)=0) PC ← PC + 2 or 3	None	1 / 2 / 3
SBIS	P, b	Skip if Bit in I/O Register is Set	if (P(b)=1) PC ← PC + 2 or 3	None	1 / 2 / 3
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then PC ← PC + k + 1	None	1 / 2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC ← PC + k + 1	None	1 / 2
BREQ	k	Branch if Equal	if (Z = 1) then PC ← PC + k + 1	None	1 / 2
BRNE	k	Branch if Not Equal	if (Z = 0) then PC ← PC + k + 1	None	1 / 2
BRCS	k	Branch if Carry Set	if (C = 1) then PC ← PC + k + 1	None	1 / 2
BRCC	k	Branch if Carry Cleared	if (C = 0) then PC ← PC + k + 1	None	1 / 2
BRSH	k	Branch if Same or Higher	if (C = 0) then PC ← PC + k + 1	None	1 / 2
BRLO	k	Branch if Lower	if (C = 1) then PC ← PC + k + 1	None	1 / 2
BRMI	k	Branch if Minus	if (N = 1) then PC ← PC + k + 1	None	1 / 2
BRPL	k	Branch if Plus	if (N = 0) then PC ← PC + k + 1	None	1 / 2
BRGE	k	Branch if Greater or Equal, Signed	if (N ⊕ V = 0) then PC ← PC + k + 1	None	1 / 2
BRLT	k	Branch if Less Than Zero, Signed	if (N ⊕ V = 1) then PC ← PC + k + 1	None	1 / 2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then PC ← PC + k + 1	None	1 / 2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then PC ← PC + k + 1	None	1 / 2
BRTS	k	Branch if T Flag Set	if (T = 1) then PC ← PC + k + 1	None	1 / 2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then PC ← PC + k + 1	None	1 / 2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then PC ← PC + k + 1	None	1 / 2
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC ← PC + k + 1	None	1 / 2

Mnemonics	Operands	Description	Operation	Flags	#Clocks
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC ← PC + k + 1	None	1 / 2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC ← PC + k + 1	None	1 / 2
DATA TRANSFER INSTRUCTIONS					
MOV	Rd, Rr	Move Between Registers	Rd ← Rr	None	1
MOVW	Rd, Rr	Copy Register Word	Rd+1:Rd ← Rr+1:Rr	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1
LD	Rd, X	Load Indirect	Rd ← (X)	None	2
LD	Rd, X+	Load Indirect and Post-Inc.	Rd ← (X), X ← X + 1	None	2
LD	Rd, -X	Load Indirect and Pre-Dec.	X ← X - 1, Rd ← (X)	None	2
LD	Rd, Y	Load Indirect	Rd ← (Y)	None	2
LD	Rd, Y+	Load Indirect and Post-Inc.	Rd ← (Y), Y ← Y + 1	None	2
LD	Rd, -Y	Load Indirect and Pre-Dec.	Y ← Y - 1, Rd ← (Y)	None	2
LDD	Rd, Y+q	Load Indirect with Displacement	Rd ← (Y + q)	None	2
LD	Rd, Z	Load Indirect	Rd ← (Z)	None	2
LD	Rd, Z+	Load Indirect and Post-Inc.	Rd ← (Z), Z ← Z+1	None	2
LD	Rd, -Z	Load Indirect and Pre-Dec.	Z ← Z - 1, Rd ← (Z)	None	2
LDD	Rd, Z+q	Load Indirect with Displacement	Rd ← (Z + q)	None	2
LDS	Rd, k	Load Direct from SRAM	Rd ← (k)	None	2
ST	X, Rr	Store Indirect	(X) ← Rr	None	2
ST	X+, Rr	Store Indirect and Post-Inc.	(X) ← Rr, X ← X + 1	None	2
ST	-X, Rr	Store Indirect and Pre-Dec.	X ← X - 1, (X) ← Rr	None	2
ST	Y, Rr	Store Indirect	(Y) ← Rr	None	2
ST	Y+, Rr	Store Indirect and Post-Inc.	(Y) ← Rr, Y ← Y + 1	None	2
ST	-Y, Rr	Store Indirect and Pre-Dec.	Y ← Y - 1, (Y) ← Rr	None	2
STD	Y+q, Rr	Store Indirect with Displacement	(Y + q) ← Rr	None	2
ST	Z, Rr	Store Indirect	(Z) ← Rr	None	2

ST	Z+, Rr	Store Indirect and Post-Inc.	$(Z) \leftarrow Rr, Z \leftarrow Z + 1$	None	2
ST	-Z, Rr	Store Indirect and Pre-Dec.	$Z \leftarrow Z - 1, (Z) \leftarrow Rr$	None	2
STD	Z+q, Rr	Store Indirect with Displacement	$(Z + q) \leftarrow Rr$	None	2
STS	k, Rr	Store Direct to SRAM	$(k) \leftarrow Rr$	None	2
LPM		Load Program Memory	$R0 \leftarrow (Z)$	None	3
LPM	Rd, Z	Load Program Memory	$Rd \leftarrow (Z)$	None	3
LPM	Rd, Z+	Load Program Memory and Post-Inc	$Rd \leftarrow (Z), Z \leftarrow Z + 1$	None	3
SPM		Store Program Memory	$(Z) \leftarrow R1:R0$	None	-
IN	Rd, P	In Port	$Rd \leftarrow P$	None	1
OUT	P, Rr	Out Port	$P \leftarrow Rr$	None	1
PUSH	Rr	Push Register on Stack	$Stack \leftarrow Rr$	None	2
POP	Rd	Pop Register from Stack	$Rd \leftarrow Stack$	None	2
BIT AND BIT-TEST INSTRUCTIONS					
SBI	P,b	Set Bit in I/O Register	$I/O(P,b) \leftarrow 1$	None	2
CBI	P,b	Clear Bit in I/O Register	$I/O(P,b) \leftarrow 0$	None	2
LSL	Rd	Logical Shift Left	$Rd(n+1) \leftarrow Rd(n), Rd(0) \leftarrow 0$	Z,C,N,V	1
LSR	Rd	Logical Shift Right	$Rd(n) \leftarrow Rd(n+1), Rd(7) \leftarrow 0$	Z,C,N,V	1
ROL	Rd	Rotate Left Through Carry	$Rd(0) \leftarrow C, Rd(n+1) \leftarrow Rd(n), C \leftarrow Rd(7)$	Z,C,N,V	1
ROR	Rd	Rotate Right Through Carry	$Rd(7) \leftarrow C, Rd(n) \leftarrow Rd(n+1), C \leftarrow Rd(0)$	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	$Rd(n) \leftarrow Rd(n+1), n=0..6$	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	$Rd(3..0) \leftarrow Rd(7..4), Rd(7..4) \leftarrow Rd(3..0)$	None	1
BSET	s	Flag Set	$SREG(s) \leftarrow 1$	SREG(s)	1
BCLR	s	Flag Clear	$SREG(s) \leftarrow 0$	SREG(s)	1
BST	Rr, b	Bit Store from Register to T	$T \leftarrow Rr(b)$	T	1
BLD	Rd, b	Bit load from T to Register	$Rd(b) \leftarrow T$	None	1
SEC		Set Carry	$C \leftarrow 1$	C	1
CLC		Clear Carry	$C \leftarrow 0$	C	1
SEN		Set Negative Flag	$N \leftarrow 1$	N	1
CLN		Clear Negative Flag	$N \leftarrow 0$	N	1
SEZ		Set Zero Flag	$Z \leftarrow 1$	Z	1
CLZ		Clear Zero Flag	$Z \leftarrow 0$	Z	1
SEI		Global Interrupt Enable	$I \leftarrow 1$	I	1
CLI		Global Interrupt Disable	$I \leftarrow 0$	I	1
SES		Set Signed Test Flag	$S \leftarrow 1$	S	1
CLS		Clear Signed Test Flag	$S \leftarrow 0$	S	1
SEV		Set Twos Complement Overflow.	$V \leftarrow 1$	V	1
CLV		Clear Twos Complement Overflow	$V \leftarrow 0$	V	1
SET		Set T in SREG	$T \leftarrow 1$	T	1
CLT		Clear T in SREG	$T \leftarrow 0$	T	1
SEH		Set Half Carry Flag in SREG	$H \leftarrow 1$	H	1

Mnemonics	Operands	Description	Operation	Flags	#Clocks
CLH		Clear Half Carry Flag in SREG	$H \leftarrow 0$	H	1
MCU CONTROL INSTRUCTIONS					

NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep function)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR/timer)	None	1
BREAK		Break	For On-Chip Debug Only	None	N/A

Ordering Information

Speed (MHz)	Power Supply	Ordering Code ⁽²⁾	Package ⁽¹⁾	Operational Range
8	2.7V - 5.5V	ATmega32L-8AU ATmega32L-8AUR ⁽³⁾ ATmega32L-8PU ATmega32L-8MU ATmega32L-8MUR ⁽³⁾	44A 44A 40P6 44M1 44M1	Industrial (-40°C to 85°C)
16	4.5V - 5.5V	ATmega32-16AU ATmega32-16AUR ⁽³⁾ ATmega32-16PU ATmega32-16MU ATmega32-16MUR ⁽³⁾	44A 44A 40P6 44M1 44M1	

Notes: 1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

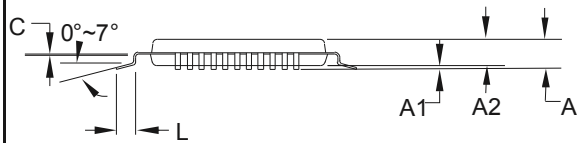
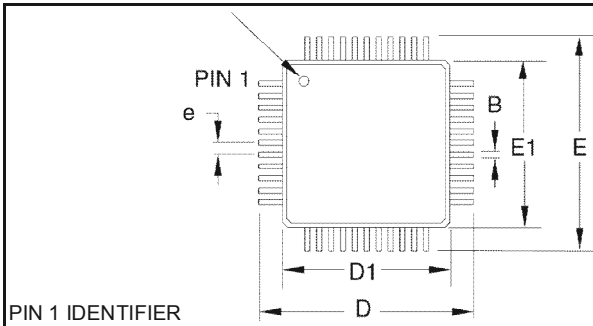
2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. Tape & Reel

Package Type	
44A	44-lead, 10 × 10 × 1.0mm, Thin Profile Plastic Quad Flat Package (TQFP)

40P6	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)
44M1	44-pad, 7 × 7 × 1.0mm, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)

Packaging Information

44A



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:

1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

2010-10-20



San Jose, CA 95131

2325 Orchard Parkway

TITLE

44A, 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)

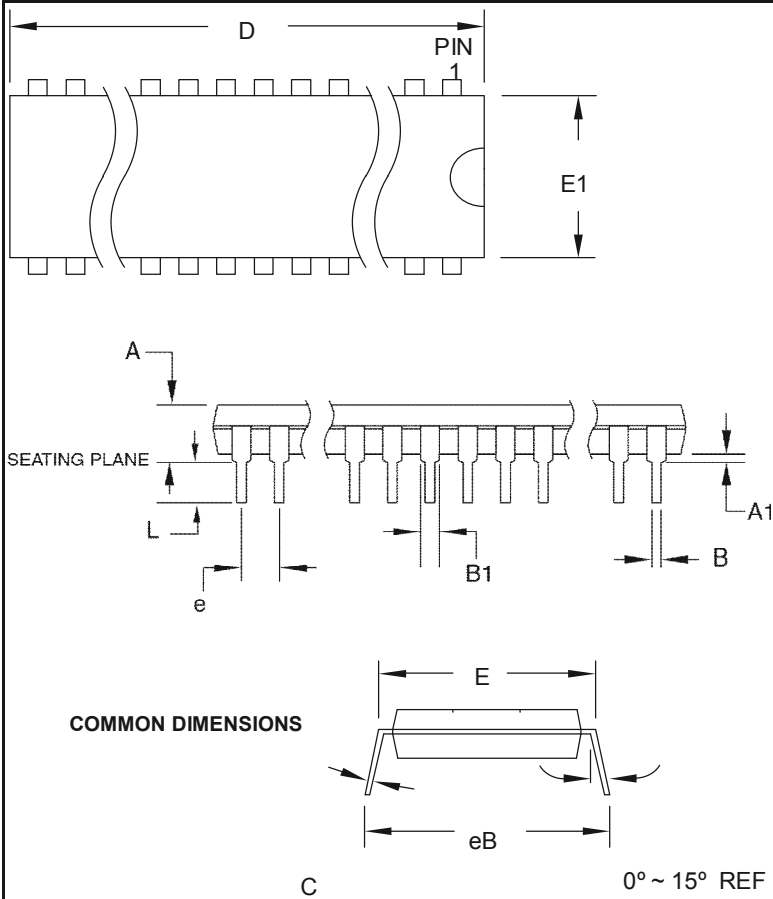
DRAWING NO.

44A

REV.

C

40P6



SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	4.826	
A1	0.381	-	-	
(Unit of Measure = mm)				
D	52.070	-	52.578	Note 2
E	15.240	-	15.875	
E1	13.462	-	13.970	Note 2
B	0.356	-	0.559	
B1	1.041	-	1.651	
L	3.048	-	3.556	
C	0.203	-	0.381	
eB	15.494	-	17.526	
e	2.540 TYP			

Notes: 1. This package conforms to JEDEC reference MS-011, Variation AC.
 2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01



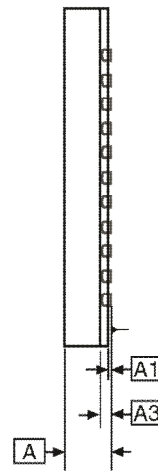
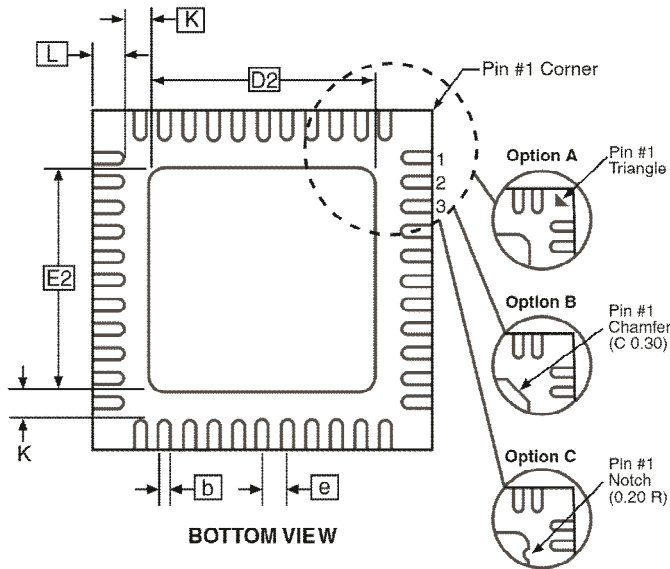
2325 Orchard
Parkway
San Jose, CA 95131

TITLE
40P6, 40-lead (0.600"/15.24 mm Wide) Plastic Dual Inline
Package (PDIP)

DRAWING NO.
40P6

REV.
B

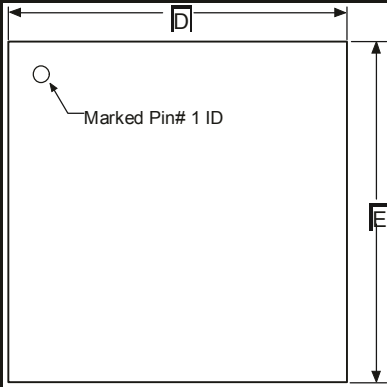
44M1



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	—	0.02	0.05	
A3	0.20 REF			
b	0.18	0.23	0.30	
D	6.90	7.00	7.10	
D2	5.00	5.20	5.40	
E	6.90	7.00	7.10	
E2	5.00	5.20	5.40	
e	0.50 BSC			
L	0.59	0.64	0.69	
K	0.20	0.26	0.41	


Note: JEDEC Standard MO-220, Fig. 1 (SAW Singulation) VKKD-3.



TOP VIEW

SEATING PLANE

9/26/08

 <p>Package Drawing Contact: packagedrawings@atmel.com</p>	<p>TITLE 44M1, 44-pad, 7 x 7 x 1.0 mm Body, Lead Pitch 0.50 mm, 5.20 mm Exposed Pad, Thermally Enhanced Plastic Very Thin Quad Flat No Lead Package (VQFN)</p>	<p>GPC ZWS</p>	<p>DRAWING NO. 44M1</p>	<p>REV. H</p>
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Errata

ATmega32, rev. A • **First Analog Comparator conversion may be delayed to F** • **Interrupts may be lost when writing the timer registers in the asynchronous timer**

- **IDCODE masks data from TDI input**
- **Reading EEPROM by using ST or STS to set EERE bit triggers unexpected interrupt request.**

1. First Analog Comparator conversion may be delayed

If the device is powered by a slow rising V_{CC} , the first Analog Comparator conversion will take longer than expected on some devices.

Problem Fix/Workaround

When the device has been powered or reset, disable then enable the Analog Comparator before the first conversion.

2. Interrupts may be lost when writing the timer registers in the asynchronous timer

The interrupt will be lost if a timer register that is synchronous timer clock is written when the asynchronous Timer/Counter register (TCNTx) is 0x00.

Problem Fix/Workaround

Always check that the asynchronous Timer/Counter register neither have the value 0xFF nor 0x00 before writing to the asynchronous Timer Control Register (TCCRx), asynchronous Timer Counter Register (TCNTx), or asynchronous Output Compare Register (OCRx).

3. IDCODE masks data from TDI input

The JTAG instruction IDCODE is not working correctly. Data to succeeding devices are replaced by all-ones during Update-DR.

Problem Fix / Workaround

- If ATmega32 is the only device in the scan chain, the problem is not visible.
- Select the Device ID Register of the ATmega32 by issuing the IDCODE instruction or by entering the Test-Logic-Reset state of the TAP controller to read out the contents of its Device ID Register and possibly data from succeeding devices of the scan chain. Issue the BYPASS instruction to the ATmega32 while reading the Device ID Registers of preceding devices of the boundary scan chain.
- If the Device IDs of all devices in the boundary scan chain must be captured simultaneously, the ATmega32 must be the first device in the chain.

4. Reading EEPROM by using ST or STS to set EERE bit triggers unexpected interrupt request.

Reading EEPROM by using the ST or STS command to set the EERE bit in the EECR register triggers an unexpected EEPROM interrupt request.

Problem Fix / Workaround

Always use OUT or SBI to set EERE in EECR.

Datasheet Revision History

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

- Changes from Rev. 2503P-07/09 to Rev. 2503Q-02/11
1. Updated **“Packaging Information” on page 333**, by replacing the package 44A by a correct one.
 2. Updated the datasheet according to the Atmel new Brand Style Guide.
 3. Updated **“Ordering Information” on page 332** to include Tape & Reel devices.

- Changes from Rev. 2503O-07/09 to Rev. 2503P-07/10
1. Inserted Note in **“Performing Page Erase by SPM” on page 251**.
 2. Note 6 and Note 7 in **Table 119 on page 290** have been removed.
 3. Updated **“Performing Page Erase by SPM” on page 251**.

- Changes from Rev. 2503N-06/08 to Rev. 2503O-07/09
1. Updated **“Errata” on page 336**.
 2. Updated the TOC with new template (version 5.10)

- Changes from Rev. 2503M-05/08 to Rev. 2503N-06/08
1. Added the note **“Not recommended for new designs” on “Features” on page 1**.

- Changes from Rev. 2503L-05/08 to Rev. 2503M-05/08
1. Updated **“Ordering Information” on page 12**:
 - Commercial ordering codes removed.
 - Non Pb-free package option removed.
 2. Removed note from Feature list in **“Analog to Digital Converter” on page 201**.
 3. Removed note from **Table 84 on page 215**.

- Changes from Rev. 2503K-08/07 to Rev. 2503L-05/08
1. Updated **“Fast PWM Mode” on page 75** in **“8-bit Timer/Counter0 with PWM” on page 69**:
 - Removed the last section describing how to achieve a frequency with 50% duty cycle waveform output in fast PWM mode.

- Changes from Rev. 2503J-10/06 to Rev. 2503K-08/07
1. Renamed **“Input Capture Trigger Source” to “Input Capture Pin Source” on page 94**.
 2. Updated **“Features” on page 1**.
 3. Added **“Data Retention” on page 6**.
 4. Updated **“Errata” on page 336**.
 5. Updated **“Slave Mode” on page 136**.

- Changes from Rev. 2503I-04/06 to Rev. 2503J-10/06**
1. Updated [“Fast PWM Mode”](#) on page 99.
 2. Updated [Table 38 on page 80](#), [Table 40 on page 81](#), [Table 45 on page 108](#), [Table 47 on page 109](#), [Table 50 on page 125](#) and [Table 52 on page 126](#).
 3. Updated typo in table note 6 in [“DC Characteristics”](#) on page 287.
 4. Updated [“Errata”](#) on page 336.

- Changes from Rev. 2503H-03/05 to Rev. 2503I-04/06**
1. Updated [Figure 1 on page 2](#).
 2. Added [“Resources”](#) on page 6.
 3. Added note to [“Timer/Counter Oscillator”](#) on page 31.
 4. Updated [“Serial Peripheral Interface – SPI”](#) on page 132.
 5. Updated note in [“Bit Rate Generator Unit”](#) on page 175.
 6. Updated [Table 86 on page 218](#).
 7. Updated [“DC Characteristics”](#) on page 287.

- Changes from Rev. 2503G-11/04 to Rev. 2503H-03/05**
1. MLF-package alternative changed to [“Quad Flat No-Lead/Micro Lead Frame Package QFN/MLF”](#).
 2. Updated [“Electrical Characteristics”](#) on page 287
 3. Updated [“Ordering Information”](#) on page 332.

- Changes from Rev. 2503F-12/03 to Rev. 2503G-11/04**
1. [“Channel”](#) renamed [“Compare unit”](#) in Timer/Counter sections, ICP renamed ICP1.
 2. Updated [Table 7 on page 29](#), [Table 15 on page 37](#), [Table 81 on page 206](#), [Table 114 on page 272](#), [Table 115 on page 273](#), and [Table 118 on page 289](#).
 3. Updated [Figure 1 on page 2](#), [Figure 46 on page 100](#).
 4. Updated [“Version”](#) on page 226.
 5. Updated [“Calibration Byte”](#) on page 258.
 6. Added section [“Page Size”](#) on page 258.
 7. Updated [“ATmega32 Typical Characteristics”](#) on page 296.
 8. Updated [“Ordering Information”](#) on page 332.

- Changes from Rev. 2503E-09/03 to Rev. 2503F-12/03**
1. Updated [“Calibrated Internal RC Oscillator”](#) on page 29.

Changes from Rev.
2503D-02/03 to
Rev. 2503E-09/03

1. Updated and changed “On-chip Debug System” to “[JTAG Interface and On-chip Debug System](#)” on page 35.
2. Updated [Table 15 on page 37](#).
3. Updated “[Test Access Port – TAP](#)” on page 219 regarding the JTAGEN fuse.
4. Updated description for Bit 7 – JTD: JTAG Interface Disable on [page 228](#).
5. Added a note regarding JTAGEN fuse to [Table 104 on page 257](#).
6. Updated Absolute Maximum Ratings* , DC Characteristics and ADC Characteristics in “[Electrical Characteristics](#)” on page 287.
7. Added a proposal for solving problems regarding the JTAG instruction IDCODE in “[Errata](#)” on page 336.

Changes from Rev.
2503C-10/02 to
Rev. 2503D-02/03

1. Added EEAR9 in EEARH in “[Register Summary](#)” on page 327.
2. Added Chip Erase as a first step in “[Programming the Flash](#)” on page 284 and “[Programming the EEPROM](#)” on page 285.
3. Removed reference to “Multi-purpose Oscillator” application note and “32 kHz Crystal Oscillator” application note, which do not exist.
4. Added information about PWM symmetry for Timer0 and Timer2.
5. Added note in “[Filling the Temporary Buffer \(Page Loading\)](#)” on page 251 about writing to the EEPROM during an SPM Page Load.
6. Added “Power Consumption” data in “[Features](#)” on page 1.
7. Added section “[EEPROM Write During Power-down Sleep Mode](#)” on page 22.
8. Added note about Differential Mode with Auto Triggering in “[Prescaling and Conversion Timing](#)” on page 204.
9. Updated [Table 89 on page 232](#).
10. Added updated “[Packaging Information](#)” on page 333.

Changes from Rev.
2503B-10/02 to
Rev. 2503C-10/02

1. Updated the “[DC Characteristics](#)” on page 287.

Changes from Rev.
2503A-03/02 to
Rev. 2503B-10/02

1. Changed the endurance on the Flash to 10,000 Write/Erase Cycles.
2. Bit nr.4 – ADHSM – in SFIOR Register removed.
3. Added the section “[Default Clock Source](#)” on page 25.
4. When using External Clock there are some limitations regards to change of fre-

- quency. This is described in [“External Clock” on page 31](#) and [Table 117 on page 289](#).
5. Added a sub section regarding OCD-system and power consumption in the section [“Minimizing Power Consumption” on page 34](#).
 6. Corrected typo (WGM-bit setting) for:
 - [“Fast PWM Mode” on page 75](#) (Timer/Counter0)
 - [“Phase Correct PWM Mode” on page 76](#) (Timer/Counter0)
 - [“Fast PWM Mode” on page 120](#) (Timer/Counter2) – [“Phase Correct PWM Mode” on page 121](#) (Timer/Counter2)
 7. Corrected [Table 67 on page 164](#) (USART).
 8. Updated V_{IL} , I_{IL} , and I_{IH} parameter in [“DC Characteristics” on page 287](#).
 9. Updated Description of OSCCAL Calibration Byte.

In the datasheet, it was not explained how to take advantage of the calibration bytes for 2, 4, and 8 MHz Oscillator selections. This is now added in the following sections:

Improved description of [“Oscillator Calibration Register – OSCCAL” on page 30](#) and [“Calibration Byte” on page 258](#).

10. Corrected typo in [Table 42](#).
11. Corrected description in [Table 45](#) and [Table 46](#).
12. Updated [Table 118](#), [Table 120](#), and [Table 121](#).
13. Added [“Errata” on page 336](#).



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