

References:-

- [1] R.Kar, V. Maheshwari, Ashis K. mal, A.K.Bhattacharjee, Power estimation for on-chip VLSI distributed RLC global interconnect using model order reduction technique, international journal of computer application, foundation of computer science, PP.92-97. Feb 2010.
- [2] M. Lajolo, A. Raghunathan, S. Dey, L. Lavagno. “Efficient Power Co-Estimation Techniques for System-on-Chip Design”, Proceedings of Design Automation and Test in Europe, March 2000, pp. 27-32.
- [3] Ghodrat, M.A.; Univ. of California, Irvine, Irvine; Lahiri, K.;Raghunathan, A, Accelerating System-on-Chip Power Analysis Using Hybrid Power Estimation, 2007.
- [4] J.Rabaey and M. Pedram (Editors), Low Power Design Methodologies. Kluwer Academic Publishers, Norwell, MA, 1996.
- [5] L.Benini and G. De Micheli, Dynamic Power Management: Design Techniques and CAD Tools. Kluwer Academic Publishers, Norwell, MA, 1997.
- [6] J.Monteiro and S. Devadas, Computer-Aided Design Techniques for Low Power Sequential Logic Circuits. Kluwer Academic Publishers, Norwell, MA, 1996.
- [7] E.Macii, M. Pedram, and F. Somenzi, “High-level power modeling, estimation, and optimization,” in Proc. Design Automation Conf., pp. 504–511, June 1997.
- [8] V.Tiwari, S. Malik, and A.Wolfe, “Power analysis of embedded software: A first step towards software power minimization,” IEEE Trans. VLSI Systems, vol. 2, pp. 437–445, Dec. 1994.

- [9] T.Sato, Y. Ootaguro, M. Nagamatsu, and H. Tago, “Evaluation of architecture-level power estimation for CMOS RISC processors,” in Proc. Symp. Low Power Electronics, pp. 44–45, Oct. 1995.
- [10] L.Benini and G. DeMicheli, “System-level power optimization: techniques and tools,” in Proc. Int. Symp. Low Power Electronics & Design, Aug. 1999.
- [11] D.Kirkovski andM. Potkonjak, “System-level synthesis of low-power hard real-time systems,” in Proc. Design Automation Conf., pp. 697–702, June 1997.
- [12] B.Dave, G. Lakshminarayana, and N. K. Jha, “COSYN: Hardwaresoftware co-synthesis of embedded systems,” in Proc. Design Automation Conf., pp. 703–708, June 1997.
- [13] Y.Li and J. Henkel, “A framework for estimating and minimizing energy dissipation of embedded HW/SW systems,” in Proc. Design Automation Conf., pp. 188–193, June 1998.
- [14] J.Henkel, “A low power hardware/software partitioning approach for core-based embedded systems,” in Proc. Design Automation Conf., pp. 122–127, June 1999.
- [15] K.Lahiri and A. Raghunathan, Power analysis of system-level on-chip communication architectures, International Conference on hardware software codesign CODES+ISSS, pp. 236-241, 2004.
- [16] Hong-Hui Chen, Tung-Chien Chen, Cheng-Yi Chiang, Liang-Gee Chen, “Power estimation scheme for low power oriented biomedical SoC extended to very deep submicron technology”, international conference on acoustics speech and signal processing (ICASSP) Conf., 2011.

- [17] Sumit Ahuja, “High level power estimation and reduction techniques for power aware hardware design”, unpublished PhD thesis, Virginia polytechnic institute and state university, May 2010.
- [18] David Y. Feinstein, Mitchell A.Thornton and Fatih Kocan, “System-on-Chip power consumption refinement and analysis”, in Proc. 6th IEEE Dallas circuits and system workshop DCAS, 2007.
- [19] Liang-Bi Chen, Tsung-Yu Ho, Chi-Hung Lin, and Ing-Jer Huang, “A real-time power analysis system for an embedded systems development platform”, in Proc. IEEE Asia-Pacific design automation Conf., Japan, Jan 2007.
- [20] Luca Benini, Robin Hodgson and Polly Siegel, “System-level power estimation and optimization” in Proc. Low power electronic and design Conf., Aug 1998.
- [21] M. Onouchi, T. Yamada, K. Morikawa, I. Mochizuki, and H. Sekine. A system-level power-estimation methodology based on IP-level modeling, power-level adjustment, and power accumulation. In ASP-DAC '06: Proceedings of the 2006 conference on Asia South Pacific design automation, pages 547–550, New York, NY, USA, 2006. ACM Press.
- [22] R.Ho, K. Mai, M. Horowitz, “The Future of wires,” Proceedings of the IEEE journal, pp. 490-504, April 2001.
- [23] J.Walrand, P. Varaiya, High-Performance Communicatio Networks, Morgan Kaufman, 2000.
- [24] T.Mudge , Power: A first-class architectural design constraint, IEEE Computer, Vol. 34, No.4, pp. 52 - 58, April 2001.

- [25] P.Gupta, L. Zhong and N. K. Jha, A high-level interconnect power model for design space exploration, International Conference on Computer Aided Design (ICCAD) , pp. 551-558, November 2003.
- [26] J.Rabaey, A. Chandrakasan and B. Nikolic , Digital Integrated Circuits , Englewood Cliffs, Prentice Hall ,NJ , 1996 .
- [27] M.Kuhlmann and S. S. Sapatnekar , Exact and efficient crosstalk estimation, IEEE Transactions on Computer-Aided Design (TCAD) , Vol. 20 , No. 7, pp.858 - 866, July 2001.
- [28] P. P. Sotiriadis and A. P. Chandrakasan, A bus energy model for deep submicron technology, IEEE Transactions on Very Large Scale Integration Systems (TVLSI) , Vol. 10 , No. 3, pp. 341-350, June 2002.
- [29] P.Kapur, G. Chandra and K. C. Saraswat, Power estimation in global interconnects and its reduction using a novel repeater optimization methodology, in Proceedings Design Automation Conference (DAC), pp. 461-466, June 2002.
- [30] D.Sylvester and C. Hu, Analytical modeling and characterization of deep submicrometer interconnect, Proceedings of IEEE journal, Vol 89, No. 5, pp. 634 - 664, May 2001.
- [31] K.Banerjee, A. Mehrotra, A. Sangiovanni-Vincentelli and C. Hu, on thermal effects in deep submicron VLSI interconnects, in Proceedings of 36th ACM Design Automation Conference (DAC), pp. 885-891, 1999.
- [32] C.Kretzschmar, A.K. Nieuwland and D. Muller, Why transition coding for power minimization of on-chip buses does not work, Design, Automation and Test in Europe Conference and Exhibition, pp. 512-517 February 16-20, 2004.

- [33] C.N.Taylor, S. Dey and Y. Zhao, Modeling and minimization of interconnect energy dissipation in nanometer technologies, in Proceedings of Design Automation Conference (DAC), pp. 754-757, June 2001.
- [34] Sudeep Pasricha, Nikil Dutt, On-Chip Communication Architectures System on Chip Interconnect, Morgan Kaufmann, 2008.
- [35] Zhonghai Lu, Design and Analysis of On-Chip Communication for Network-on-Chip Platforms, PhD thesis, Stockholm's Royal Institute of Technology, 2007.
- [36] Terry Tao Ye, On-chip multiprocessor communication network design and analysis, PhD thesis, Stanford University, December 2003.

Appendix:

```
clc
clear
close all
c=135.78;
r=98.02;
l=14.2*10^3;
M=50;
f=1.68*10^9;
n=1;
xline=19.04;
xinter=136.671;
rint=98.02;
xint=xline+2*xinter;
ro=rand(1,1);
xo=rand(1,1);
h=sqrt((ro*xint)/(xo*rint));
k=sqrt((0.4*(rint*xint))/(0.7*(ro*xo)));
zo=sqrt(l/c);
zrep=h*k*zo;
pvia=0.6*10.^-3;
for i=1:M;
x=rand(50,1);
psiload=rand(50,1);
psidesel=rand(50,1);
psiHdin=rand(50,1);
psidrive=rand(50,1);
psislavesel=rand(50,1);
psirepsel=rand(50,1);
psisel=rand(50,1);
psiaddress1=rand(50,1);
psidatasel=rand(50,1);
psinopoport=rand(50,1);
psiarb=rand(50,1);
psinextarb=rand(50,1);
psinextdesel=rand(50,1);
psidesel2=rand(50,1);
```

```

%dissipated energy in input stage
Einp=7.78+3.81*psiload+2.6*psidesel+0.96*psiHdin+3.27*psidrive;
%dissipated energy in decoder
Edec=0.47+3.04*psislavesel+2.17*psirepsel+0.13*psiHdin+0.38*psisel;
%dissipated energy in output stage
Eout=0.72+2.61*psiaddress1+1.53*psidatasel+0.14*psiHdin+1.48*psinoport;
%dissipated energy in arbiter
Earb=0.65+(0.76+n*0.3)*psiarb+0.6*psinextarb+(0.34+n*0.48)*psidesel2+0.52*psi
nextdesel;
%dissipated energy in wire
D=((x*((r*sqrt(c*(2*l)-c*r^3))+sqrt(c*r))/((1-c)*r^2)) );
G=(r*c)^2*((c*(2*l-c*r^2))/(r^2+sqrt(c*(2*(l-c)*r^2))) );
If (Einp < 13) {
Ewire=(G*exp(-D))*10^-12;
} else {
vdd=1.1;
vd=vdd.^2;
pi=randi(20,[50,1]);
vri=rand(50,1);
prep=zrep*vd*f*pi*50+pvia*vri;
pvias=pvia*10;
psw=rand(50,1);
ptotalinwire=(psw+prep+pvias)*10.^-17;
}
}

avgEarb=mean(Earb);
avgEinp=mean(Einp);
avgEdec=mean(Edec);
avgEout=mean(Eout);
avgEwire=mean(Ewire);
avgpowertotalwire=mean(ptotalinwire);
powercomparison=[avgEarb;avgEinp;avgEdec;avgEout;real(avgEwire)];
end

```