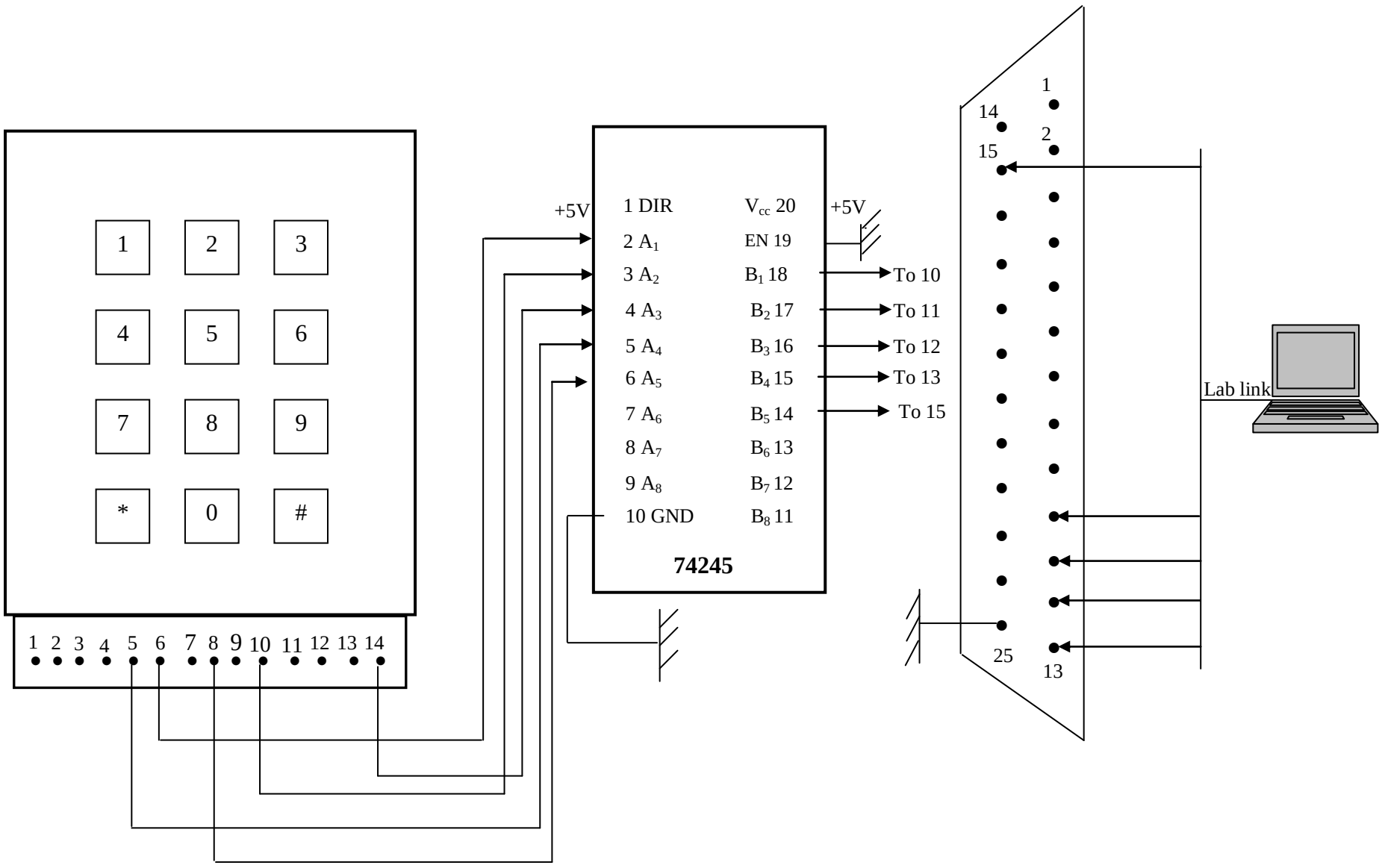

Figure 4.4 design circuit