

DEDICATION

I DEDICATE THIS WORK TO:

- My parents IBRAHIM & FATIMA who introduced me to the joy of reading from birth, enabling such study to take place today.
- To all those who directed me to the way studying and put me on the right study tract.
- To those who told me about their experiences & experiments.

ACKNOWLEDGEMENTS

First, praise is to ALLAH, the first cherisher and sustainer of the worlds. Acknowledgements here are more than a decorative ritual, the teachers, Sudan University of Science & Technology, Alzaeim Alazhari University; I'm indebted to all of them because of their support and device. They were all patient and generous in helping.

Special acknowledgement to Dr. Abd Alrasol Jabar Alzubaidy who made the completion of this work

possible in the first place by this advice and by the generous aid that he has offered to me. He has also been kind enough to follow me preparing the manuscript and to make constructive.

ABSTRACT

Major concepts of the computer buses were explained in this research. Features and characteristics for each type of these computer buses besides their development along with different computer generations were discussed. A comparison between the different buses was done.

An elaborated study of PCI local bus was implemented, where the main characteristics and features of PCI Bus were identified in details of pins layout also configuring and addressing methods of PCI Bus.

There is a scientific circuit which simulate the card inserting inside the Bus. A program using the C language read the EPROM (Card ROM) which includes the card information.

تجريد

هذا البحث يقدم شرح مؤجز لمعظم أنواع الناقل المستخدمة في الحاسب موضحاً خصائص ومميزات كل نوع وتطورها مع أجيال الحاسب مع عقد مقارنة بين أهمها. وتناول الناقل المحلي ال PCI بشي من التفصيل حيث يتم التعرف من خلاله على مميزات وخصائص الناقل مع تفصيل لكل المداخل والمخارج مع التطرق لكيفية العنونة والتهيئة والإعداد .

وصممت دائرة عملية هي تحاكي وضع كارت من النوع PCI يتم التعرف عليه من خلال برنامج كتب بلغة ال C وذلك عبر قراءة ذاكرة ال EPROM الموجودة داخل الكارت في عملية محاكاة لما يحدث في عملية Plug & Play .

Table of contents

| Topics | Page No. |
|-------------------|----------|
| Dedication | I |
| Acknowledgment | II |
| Abstract | III |
| تجربده | IV |
| Table of contents | V |
| List of Tables | VI |
| List of Figures | IX |
| Abbreviation | X |

Chapter One -Introduction

| | |
|------------------------------------|---|
| 1.1 Introduction | 1 |
| 1.2 The Computer Bus | 1 |
| 1.3 Bus Taxonomy | 3 |
| 1.4 ISA Drawback | 4 |
| 1.5 The VESA Local Bus | 5 |
| 1.6 Introducing PCI | 6 |
| 1.7 The PCI Special Interest Group | 8 |
| 1.8 Research Outline | 9 |

Chapter Two -Computer busses

| | |
|-----------------------|----|
| 2.1 Overview | 10 |
| 2.2 The S-100 | 12 |
| 2.3 ISA | 14 |
| 2.4 MCA | 17 |
| 2.5 EISA | 19 |
| 2.6 MCA vs. EISA | 21 |
| 2.7 Local Bus | 22 |
| 2.8 VL-Bus | 23 |
| 2.9 PCI | 26 |
| 2.10 VL vs. PCI bus | 28 |
| 2.11 Peripheral buses | 28 |
| 2.12 SCSI | 29 |
| 2.13 IDE | 30 |
| 2.14 SCSI Vs EIDE | 31 |

Chapter Three - PCI Local Bus

| | |
|---|----|
| 3.1 PCI Overview | 32 |
| 3.2 PCI Bus Protocol | 33 |
| 3.3 PCI Signal Descriptions | 36 |
| 3.3.1 System Pins | 36 |
| 3.3.2 Address and Data Pins | 37 |
| 3.3.3 Interface Control Pins | 39 |
| 3.3.4 Arbitration Pins (Initiator Only) | 41 |
| 3.3.5 Error Reporting Pins | 42 |
| 3.3.6 Interrupt Pins | 43 |
| 3.3.7 Cache Support Pins (Optional) | 43 |

| | |
|--|----|
| 3.3.8 Additional Pins | 44 |
| 3.3.9 64-Bit Bus Extension Pins (Optional) | 45 |
| 3.3.10 JTAG/Boundary Scan Pins (Optional) | 46 |
| 3.4 Plug and Play Configuration | 46 |
| 3.4.1 Background | 46 |
| 3.4.2 Configuration Address Space | 47 |
| 3.4.3 Configuration Transactions | 47 |
| 3.4.4 Driving IDSEL | 49 |
| 3.4.5 Configuration Header — Type 0 | 49 |
| 3.4.6 Bridge Types | 54 |
| 3.4.7 Configuration Address Types | 56 |

Chapter Four - Hardware Design

| | |
|------------------------------|----|
| 4.1 Introduction | 61 |
| 4.2 Components used | 61 |
| 4.3 Parallel port | 61 |
| 4.4 Programming the register | 63 |
| 4.4 Design steps | 64 |
| 4.5 Memory chip | 67 |
| 4.5.1 Types of ROM | 67 |
| 4.5.2 EPROM Speed | 69 |
| 4.5.3 EPROM Size rating | 69 |
| 4.5.4 Atypical EPROM pinout | 70 |
| 4.5.5 Programming an EPROM | 71 |

Chapter Five - Software

| | |
|--------------------|----|
| 5.1 Introduction: | 73 |
| 5.2 FLOW CHART. | 73 |
| 5.3 MAIN PROGRAM | 74 |
| 5.4 HOW TO OPERATE | 78 |

Chapter Six Conclusion and RECOMMENDATION

| | |
|--------------------|----|
| 6.1 Conclusion | 80 |
| 6.3 Recommendation | 80 |
| References | 81 |
| WEBS | 81 |

Appendix

Appendix (A) Complete System

Appendix (B) SN74LS245, OCTAL BUS TRANSCEIVERS, WITH 3-TATE
OUTPUTS

Appendix (C) (27C16)16,384-Bit (2048 x 8) UV Erasable
CMOS PROM

LIST OF TABLES

| Table | Description | .Page No |
|-------|--|----------|
| 1-1 | Bus parameters 4 | 4 |
| 2-1 | S-100 board feature | 11 |
| 2-2 | MCA vs. EISA | 21 |
| 2-3 | SCSI types | 30 |
| 3-1 | Bus command codes | 38 |
| 3-2 | Encoding PRSNT[1:2] signals | 44 |
| 4-1 | Pinout of parallel port | 62 |
| 4-2 | Data Register | 63 |
| 4-3 | Status Register | 64 |
| 4-4 | Control Register | 64 |
| 4-5 | (From DB-25 to IC No.1 (SN74245 | 64 |
| 4-6 | From DB-25 to IC No.2 (SN74245) | 66 |
| 4-7 | (From IC No.1 (SN74245) to IC No.3 (EPROM 2716 | 66 |
| 4-8 | From IC No.2 (SN74245) to IC No.3 (EPROM 2716) | 67 |

List of Figures

| Figure | Description | Page No. |
|--------|--|----------|
| 1.1 | Functional diagram of a computer bus | 2 |
| 1.2 | Functional diagram of the VL Bus | 5 |
| 3-1 | PCI signal | 36 |
| 3-2 | x86 configuration address. | 48 |
| 3-3 | Asserting IDSEL. | 49 |
| 3-4 | Type 0 configuration header. | 50 |
| 3-5 | Configuration Command Register. | 51 |
| 3-6 | Configuration Status Register. | 52 |
| 3-7 | Built-in self-test (BIST) register. | 53 |
| 3-8 | PCI bridge hierarchy. | 54 |
| 3-9 | PCI bridge structure. | 56 |
| 3-10 | Configuration address types. | 57 |
| 3-11 | Configuration space header, Type 1. | 57 |
| 3-12 | Address filtering with base and limit registers. | 59 |
| 3-13 | Memory base and limit registers. | 59 |
| 3-14 | I/O base and limit registers. | 60 |
| 3-15 | Prefetchable base and limit registers. | 60 |
| 4-1 | Parallel port | 62 |
| 4-2 | system design | 65 |
| 4-3 | Work space | 71 |
| 4-4 | Device and write the program | 72 |
| 5-1 | Flow chart | 73 |
| 5-2 | First screen of the program | 78 |
| 5-3 | Second screen of the program | 79 |

Abbreviation

| | |
|---------|---|
| ANSI | American National Standards Institute |
| ASIC | Application-specific integrated circuit |
| AT | Advanced Technology |
| BIOS | Basic Input Output System |
| BMIC | Bus Master Interface Chip |
| CD-ROM | Compact Disk - Read Only Memory |
| CPU | Central Processing Unit |
| DAC | Dual Address Cycles |
| DB-25 | D-subminiature-25 |
| DIP | Dual in-line Package |
| DMA | Direct Memory Access |
| DRAM | Dynamic Random Access Memory |
| DWORD | Double WORD |
| EEPROM | Electrically Erasable Programmable Read Only Memory |
| EIDE | Enhanced Integrated Drive Electronics |
| EISA | Extended Industry Standard Architecture |
| EPROM | Erasable Programmable Read Only Memory |
| FIFO | First In First Out |
| GPIO | General Purpose Interface Bus |
| I/O | Input |
| IC | Integrated Circuit |
| ID | Identification |
| IDE | Integrated Drive Electronics |
| IEEE | Institute of Electrical and Electronics Engineers |
| IRQ | interrupt ReQuest |
| ISA | Industry Standard Architecture |
| LAN | Local Area Network |
| LPT | Line Print Terminal |
| LSB | Least Significant Byte |
| MCA | Micro Channel Architecture |
| MTTR | Mean Time To Repair |
| OEM | Original Equipment Manufacturer |
| OTPROM | One Time Programmable Read Only Memory |
| PC | Personal Computer |
| PCI | Peripheral Component Interconnect |
| PCI SIG | <u>PCI Special Interest Group</u> |
| PCI-X | Peripheral Component Interconnect-eXtended |
| PROM | Programmable Read Only Memory |
| RAID | Redundant Array of Inexpensive Disks |
| RISC | Reduced Instruction Set Computer |
| ROM | Read Only Memory |
| SCSI | Small Computer Systems Interface |
| SPP | Standard Parallel Port |
| SVGA | Super Video Graphics Array |
| TTL | Transistor-transistor logic |

| | |
|------|---|
| USB | Universal Serial Bus |
| UV | Ultra Violet |
| VESA | Video Electronics Standards Association |
| VGA | Video Graphics Array |
| VL | VESA Local bus |
| XT | eXtended Technology |