

Features

- Complete DTMF Receiver
- Low power consumption
- Internal gain setting amplifier
- Adjustable guard time
- Central office quality
- Power-down mode
- Inhibit mode
- Backward compatible with MT8870C/MT8870C-1

ISSUE 5

March 1997

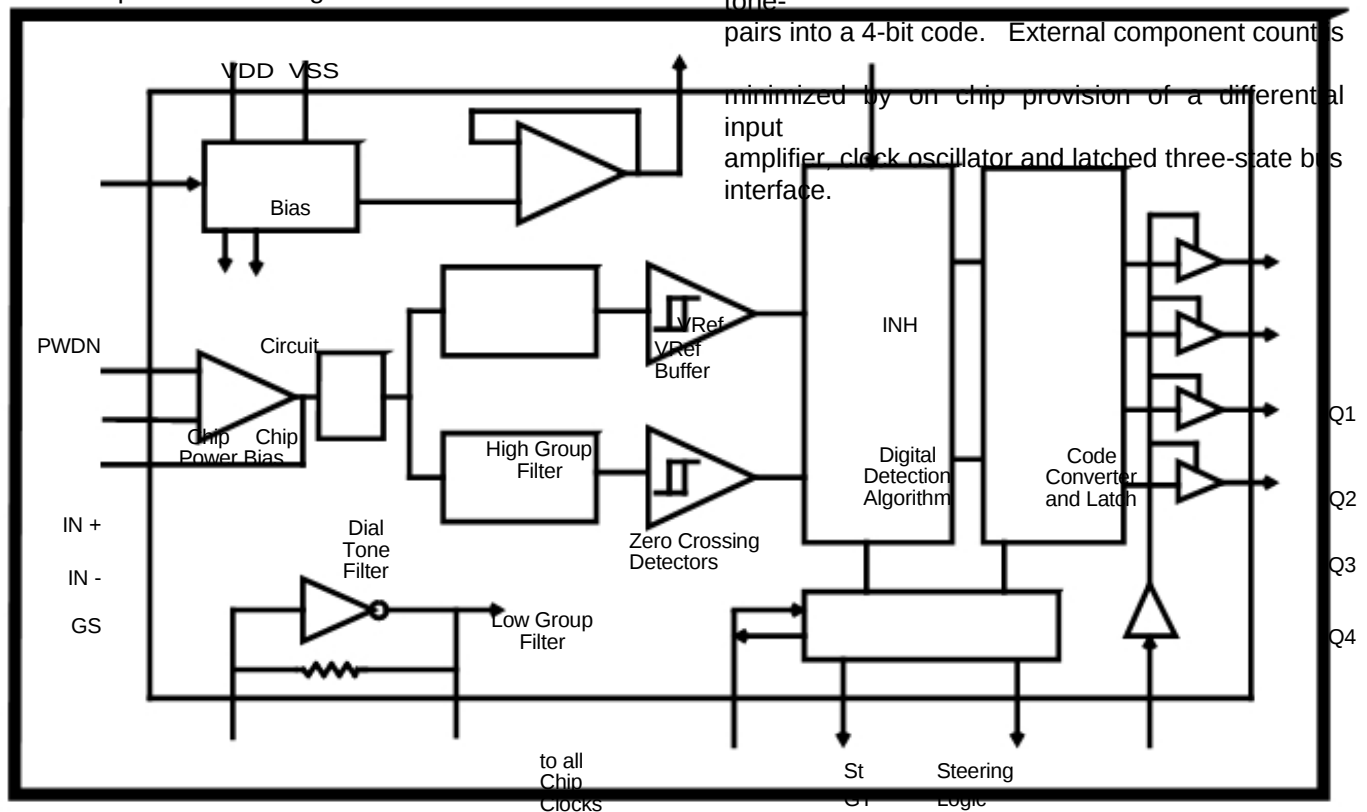
Ordering Information

MT8870DE/DE-1	18 Pin Plastic DIP
MT8870DS/DS-1	18 Pin SOIC
MT8870DN/DN-1	20 Pin SSOP
-40 °C to +85 °C	

Description

The MT8870D/MT8870D-1 is a complete DTMF receiver integrating both the bandsplit filter and digital decoder functions. The filter section uses switched capacitor techniques for high and low group filters; the decoder uses digital counting techniques to detect and decode all 16 DTMF tone-pairs into a 4-bit code. External component counts

is minimized by on chip provision of a differential input amplifier, clock oscillator and latched three-state bus interface.



OSC1

OSC2

St/GT

Est

STD

TOE

Figure 1 - Functional Block Diagram

IN+	1	18	VDD
IN-	2	17	St/GT
GS	3	16	ESt
VRef	4	15	StD
INH	5	14	Q4
PWDN	6	13	Q3
OSC1	7	12	Q2
OSC2	8	11	Q1
VSS	9	10	TOE

18 PIN PLASTIC DIP/SOIC

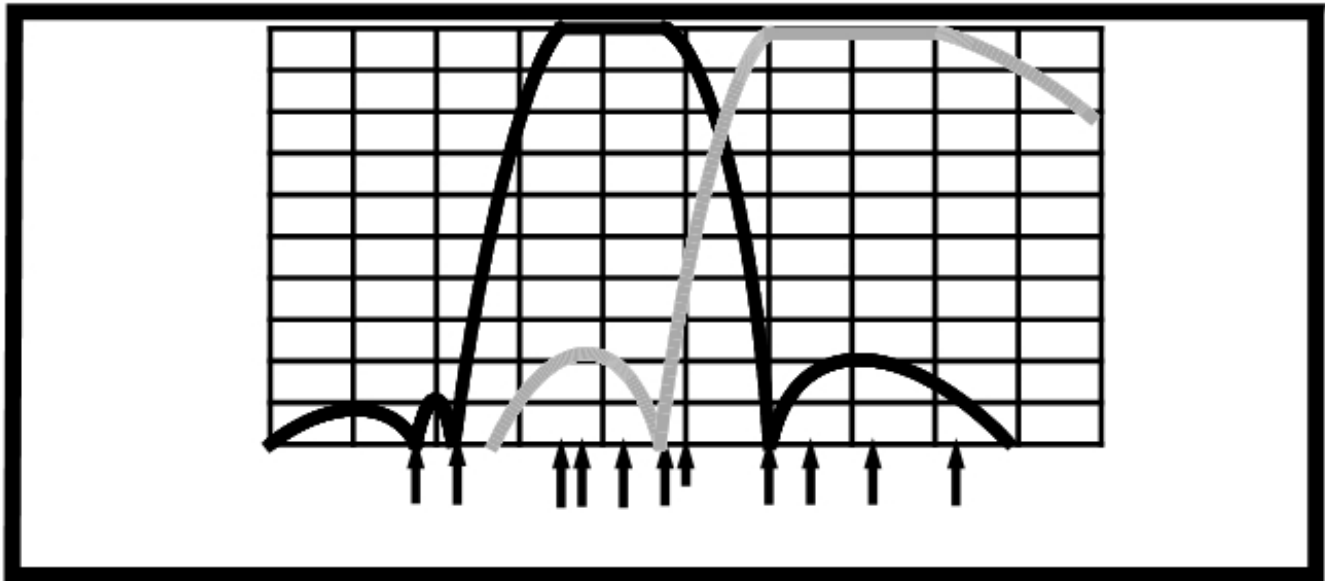
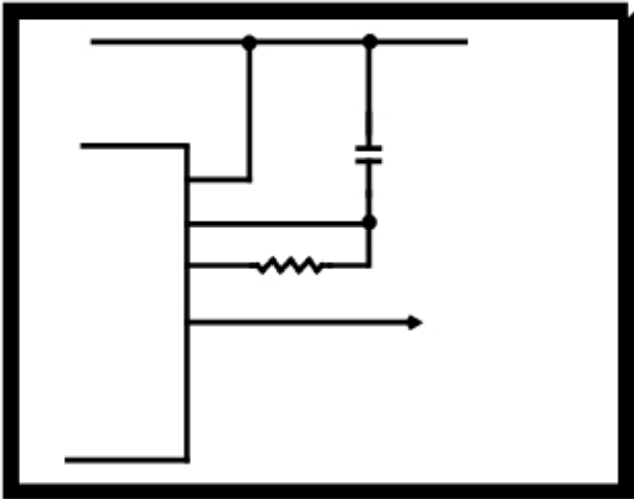
IN+	1	20	VDD
IN-	2	19	St/GT
GS	3	18	ESt
VRef	4	17	StD
INH	5	16	NC
PWDN	6	15	Q4
NC	7	14	Q3
OSC1	8	13	Q2
OSC2	9	12	Q1
VSS	10	11	TOE

20 PIN SSOP

Figure 2 - Pin Connections

Pin Description

Pin #	Name	Description
18 20		
1 1	IN+	Non-Inverting Op-Amp (Input).
2 2	IN-	Inverting Op-Amp (Input).
3 3	GS	Gain Select. Gives access to output of front end differential amplifier for connection of feedback resistor.
4 4	VRef	Reference Voltage (Output). Nominally $V_{DD}/2$ is used to bias inputs at mid-rail (see Fig. 6 and Fig. 10).
5 5	INH	Inhibit (Input). Logic high inhibits the detection of tones representing characters A, B, C and D. This pin input is internally pulled down.
6 6	PWDN	Power Down (Input). Active high. Powers down the device and inhibits the oscillator. This pin input is internally pulled down.
7 8	OSC1	Clock (Input).
8 9	OSC2	Clock (Output). A 3.579545 MHz crystal connected between pins OSC1 and OSC2 completes the internal oscillator circuit.
9 10	VSS	Ground (Input). 0V typical.
10 11	TOE	Three State Output Enable (Input). Logic high enables the outputs Q1-Q4. This pin is pulled up internally.
11- 12- 14 15	Q1-Q4	Three State Data (Output). When enabled by TOE, provide the code corresponding to the last valid tone-pair received (see Table 1). When TOE is logic low, the data outputs are high impedance.
15 17	StD	Delayed Steering (Output). Presents a logic high when a received tone-pair has been registered and the output latch updated; returns to logic low when the voltage on St/GT falls below V_{TSt} .
16 18	ESt	Early Steering (Output). Presents a logic high once the digital algorithm has detected a valid tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.
17 19	St/GT	Steering Input/Guard time (Output) Bidirectional. A voltage greater than V_{TSt} detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V_{TSt} frees the device to accept a new tone pair. The GT output acts to reset the external steering time-constant; its state is a function of ESt and the voltage on St.
18 20	VDD	Positive power supply (Input). +5V typical.
7, 16	NC	No Connection.



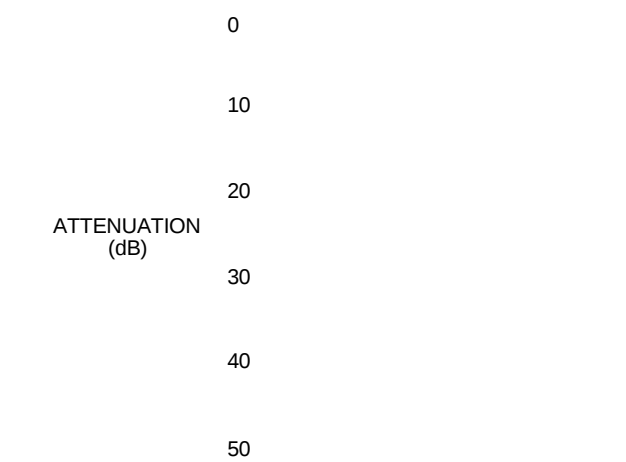
consumption and high performance. Its architecture consists of a bandsplit filter section, which separates the high and low group tones, followed by a digital counting section which verifies the frequency and duration of the received tones before passing the corresponding code to the output bus.

Filter Section

Separation of the low-group and high group tones is achieved by applying the DTMF signal to the inputs of two sixth-order switched capacitor bandpass filters, the bandwidths of which correspond to the low and high group frequencies. The filter section also incorporates notches at 350 and 440 Hz for exceptional dial tone rejection (see Figure 3). Each filter output is followed by a single order switched capacitor filter section which smooths the signals prior to limiting. Limiting is performed by high-gain comparators which are provided with hysteresis to prevent detection of unwanted low-level signals. The outputs of the comparators provide full rail logic swings at the frequencies of the incoming DTMF signals.

Decoder Section

Following the filter section is a decoder employing digital counting techniques to determine the frequencies of the incoming tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation by extraneous signals such as voice while



-CMOS MT8870D/MT8870D-1

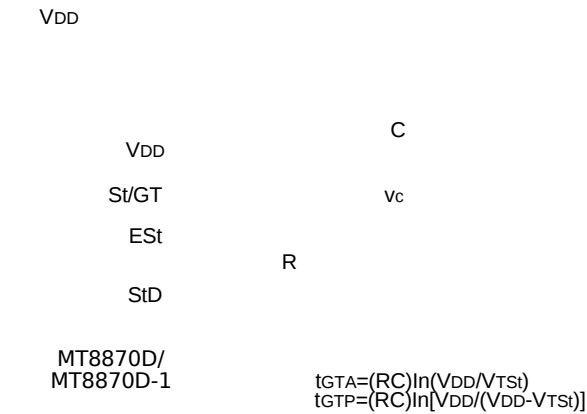


Figure 4 - Basic Steering Circuit

providing tolerance to small frequency deviations and variations. This averaging algorithm has been developed to ensure an optimum combination of immunity to talk-off and tolerance to the presence of interfering frequencies (third tones) and noise. When the detector recognizes the presence of two valid tones (this is referred to as the “signal condition” in some industry specifications) the “Early Steering” (ESt) output will go to an active state. Any subsequent loss of signal condition will cause ESt to assume an inactive state (see “Steering Circuit”).

Steering Circuit

Before registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as character recognition condition). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes v_c (see Figure 4) to rise as the capacitor discharges. Provided signal

PRECISE DIAL TONES
X=350 Hz Y=440 Hz
DTMF TONES
A=697 Hz B=770 Hz C=852 Hz D=941 Hz E=1209 Hz F=1336 Hz G=1477 Hz H=1633 Hz

X Y A B C D E F G H
FREQUENCY (Hz)

Figure 3 - Filter Response

validation period (t_{GTP}), v_c reaches the threshold (V_{TSt}) of the steering logic to register the tone pair, latching its corresponding 4-bit code (see Table 1) into the output latch. At this point the GT output is activated and drives v_c to V_{DD} . GT continues to drive high as long as ESt remains high. Finally, after a short delay to allow the output latch to settle, the delayed steering output flag (StD) goes high, signalling that a received tone pair has been registered. The contents of the output latch are made available on the 4-bit output bus by raising the three state control input (TOE) to a logic high. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (dropout) too short to be considered a valid pause. This facility, together with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

Guard Time Adjustment

In many situations not requiring selection of tone duration and interdigital pause, the simple steering circuit shown in Figure 4 is applicable. Component values are chosen according to the formula:

$$t_{REC} = t_{DP} + t_{GTP}$$

$$t_{ID} = t_{DA} + t_{GTA}$$

The value of t_{DP} is a device parameter (see Figure 11) and t_{REC} is the minimum signal duration to be recognized by the receiver. A value for C of 0.1 μF is

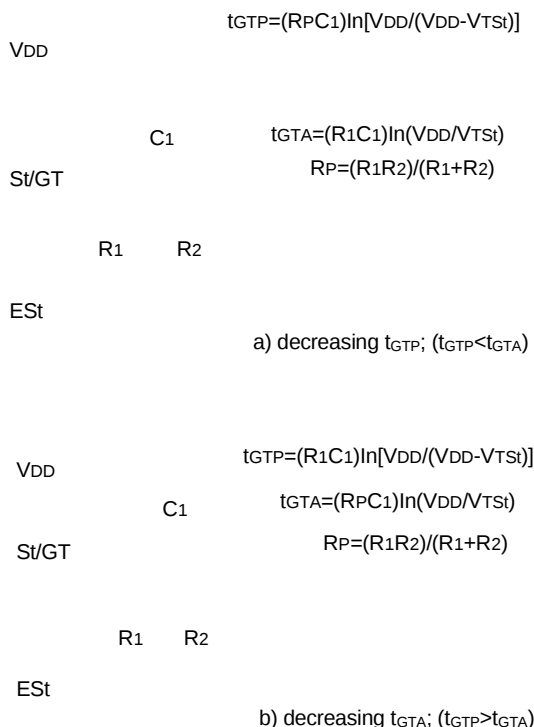


Figure 5 - Guard Time Adjustment

Digit	TOE	INH	ESt	Q4	Q3	Q2	Q1
ANY	L	X	H	Z	Z	Z	Z
1	H	X	H	0	0	0	1
2	H	X	H	0	0	1	0
3	H	X	H	0	0	1	1
4	H	X	H	0	1	0	0
5	H	X	H	0	1	0	1
6	H	X	H	0	1	1	0
7	H	X	H	0	1	1	1
8	H	X	H	1	0	0	0
9	H	X	H	1	0	0	1
0	H	X	H	1	0	1	0
*	H	X	H	1	0	1	1
#	H	X	H	1	1	0	0
A	H	L	H	1	1	0	1
B	H	L	H	1	1	1	0
C	H	L	H	1	1	1	1
D	H	L	H	0	0	0	0
A	H	H	L	undetected, the output code will remain the same as the previous detected code			
B	H	H	L				
C	H	H	L				
D	H	H	L				

Table 1. Functional Decode Table

L=LOGIC LOW, H=LOGIC HIGH, Z=HIGH IMPEDANCE X = DON'T CARE

recommended for most applications, leaving R to be selected by the designer.

Different steering arrangements may be used to select independently the guard times for tone present (t_{GTP}) and tone absent (t_{GTA}). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and interdigital pause. Guard time adjustment also allows the designer to tailor system parameters such as talk off and noise immunity. Increasing t_{REC}

improves talk-off performance since it reduces the probability that tones simulated by speech will maintain signal condition long enough to be registered. Alternatively, a relatively short t_{REC} with

a long t_{DO} would be appropriate for extremely noisy environments where fast acquisition time and immunity to tone drop-outs are required. Design information for guard time adjustment is shown in Figure 5.

oscillator and the functions of the filters.

Inhibit mode is enabled by a logic high input to the pin 5 (INH). It inhibits the detection of tones representing characters A, B, C, and D. The output code will remain the same as the previous detected code (see Table 1).

Differential Input Configuration

The input arrangement of the MT8870D/MT8870D-1 provides a differential-input operational amplifier as well as a bias source (V_{Ref}) which is used to bias the inputs at mid-rail. Provision is made for connection of a feedback resistor to the op-amp output (GS) for adjustment of gain. In a single-ended configuration,

the input pins are connected as shown in Figure 10 with the op-amp connected for unity gain and V_{Ref} biasing the input at $1/2V_{DD}$. Figure 6 shows the differential configuration, which permits the adjustment of gain with the feedback resistor R_5 .

Crystal Oscillator

The internal clock circuit is completed with the addition of an external 3.579545 MHz crystal and is normally connected as shown in Figure 10 (Single-Ended Input Configuration). However, it is possible to configure several MT8870D/MT8870D-1 devices employing only a single oscillator crystal. The oscillator output of the first device in the chain is coupled through a 30 pF capacitor to the oscillator input (OSC1) of the next device. Subsequent devices are connected in a similar fashion. Refer to Figure 7 for details. The problems associated with unbalanced loading are not a concern with the arrangement shown, i.e., precision balancing capacitors are not required.

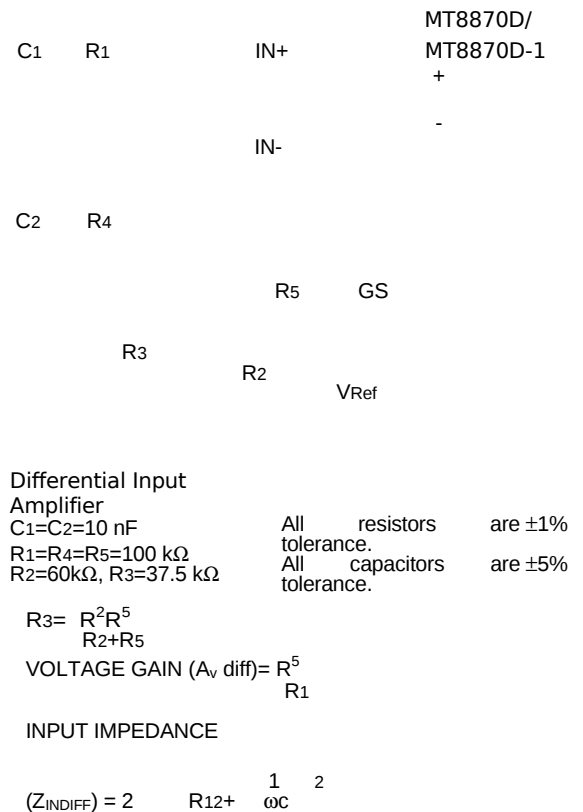


Figure 6 - Differential Input Configuration

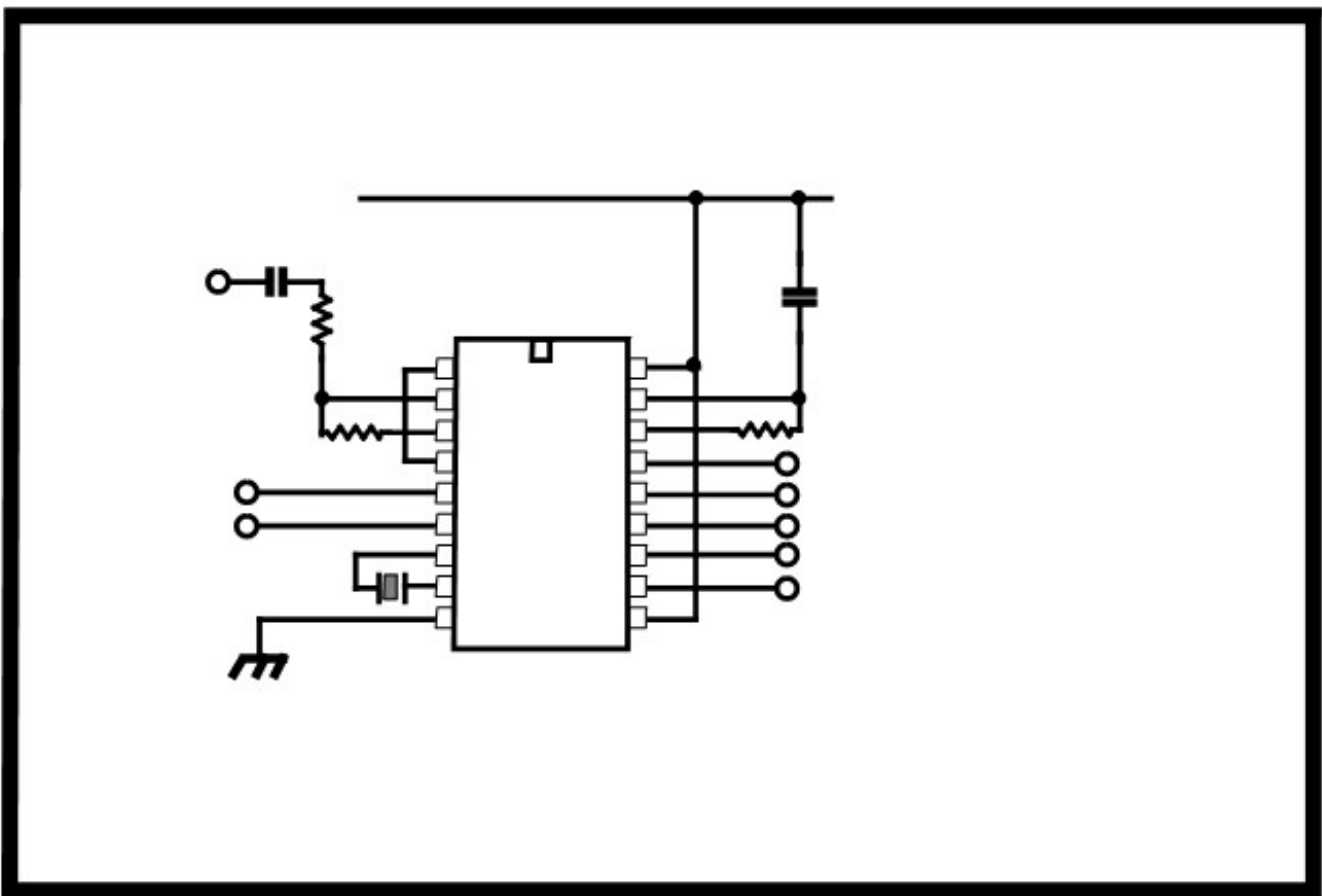
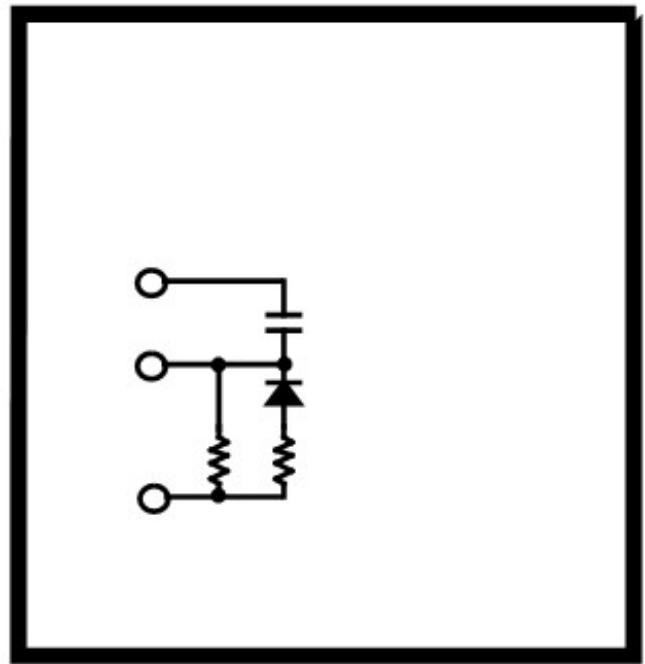


Figure 7 - Oscillator Connection

Parameter	Unit	Resonator
R1	Ohms	10.752
L1	mH	.432
C1	pF	4.984
C0	pF	37.915
Qm	-	896.37
Δf	%	$\pm 0.2\%$

Table 2. Recommended Resonator Specifications

Note: Qm=quality factor of RLC model, i.e., $1/2\pi f/R1C1$.



MT8870D/MT8870D-1 ISO²-CMOS

Applications

The circuit shown in Fig. 9 illustrates the use of MT8870D-1 device in a typical receiver system. BT Spec defines the input signals less than -34 dBm as the non-operate level. This condition can be attained by choosing a suitable values of R_1 and R_2 to provide 3 dB attenuation, such that -34 dBm input signal will correspond to -37 dBm at the gain setting pin GS of MT8870D-1. As shown in the diagram, the component values of R_3 and C_2 are the guard time requirements when the total component tolerance is 6%. For better performance, it is recommended to use the non-symmetric guard time circuit in Fig. 8.

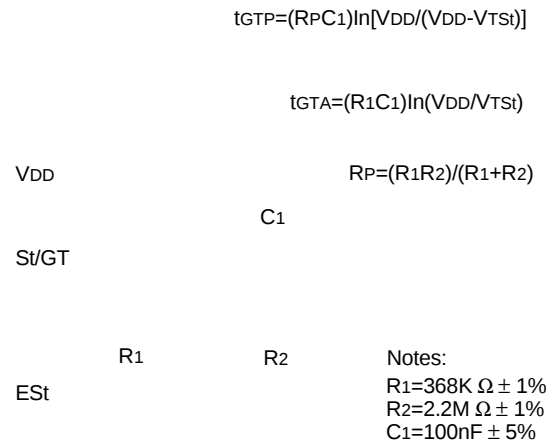


Figure 8 - Non-Symmetric Guard Time Circuit

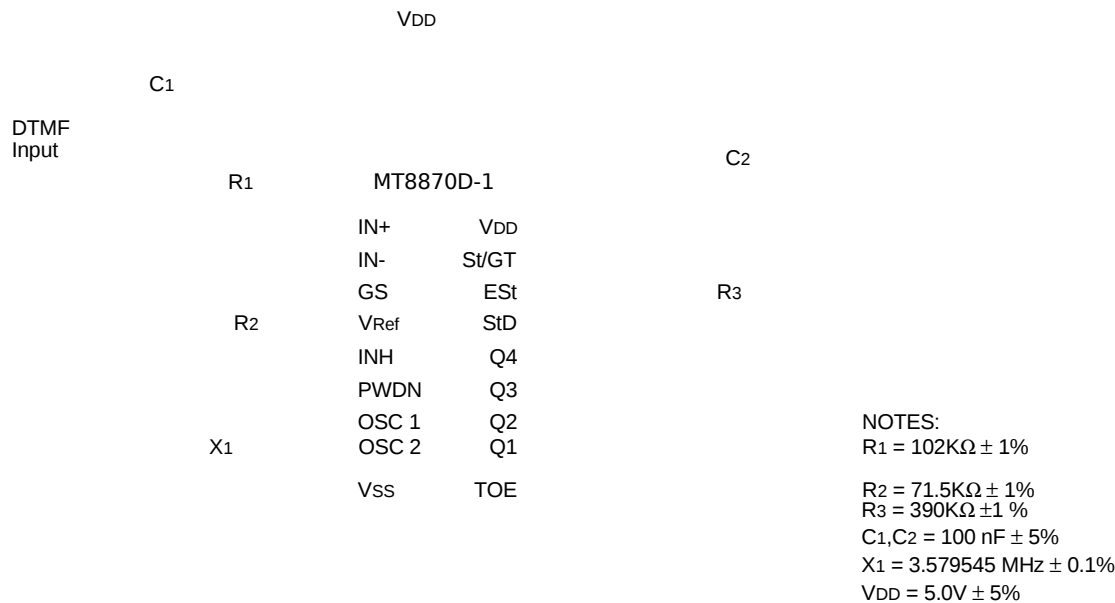


Figure 9 - Single-Ended Input Configuration for BT or CEPT Spec

	Parameter	Symbol	Min	Max	Units
1	DC Power Supply Voltage	V _{DD}		7	V
2	Voltage on any pin	V _I	V _{SS} -0.3	V _{DD} +0.3	V
3	Current at any pin (other than supply)	I _I		10	mA
4	Storage temperature	T _{STG}	-65	+150	°C
5	Package power dissipation	P _D		500	mW

† Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
Derate above 75 °C at 16 mW / °C. All leads soldered to board.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Parameter	Sym	Min	Typ [‡]	Max	Units	Test Conditions
1	DC Power Supply Voltage	V _{DD}	4.75	5.0	5.25	V	
2	Operating Temperature	T _O	-40		+85	°C	
3	Crystal/Clock Frequency	f _c		3.579545		MHz	
4	Crystal/Clock Freq.Tolerance	Δf _c		±0.1		%	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics V_{DD}=5.0V± 5%, V_{SS}=0V, -40°C ≤ T_O ≤ +85°C, unless otherwise stated.

	Characteristics	Sym	Min	Typ [‡]	Max	Units	Test Conditions
		I _{DDQ}		10	25	μA	PWDN=V _{DD}
1	S Standby supply current	I _{DD}		3.0	9.0	mA	
2	P Operating supply current						
3	P Power consumption	P _O		15		mW	f _c =3.579545 MHz
	L						
4	Y High level input	V _{IH}	3.5			V	V _{DD} =5.0V
5	Low level input voltage	V _{IL}			1.5	V	V _{DD} =5.0V
6							
7	I Input leakage current	I _{IH} /I _{IL}		0.1		μA	V _{IN} =V _{SS} or V _{DD}
8	N Pull up (source) current	I _{SO}		7.5	20	μA	TOE (pin 10)=0, V _{DD} =5.0V
	P						
9	T Pull down (sink) current	I _{SI}		15	45	μA	INH=5.0V, PWDN=5.0V, V _{DD} =5.0V
	S						
10	Input impedance (IN+, IN-)	R _{IN}		10		MΩ	@ 1 kHz
11	Steering threshold voltage	V _{TSt}	2.2	2.4	2.5	V	V _{DD} = 5.0V
12	Low level output voltage	V _{OL}			V _{SS} +0.03	V	No load
13	High level output voltage	V _{OH}	V _{DD} -0.03			V	No load
14	Output low (sink) current	I _{OL}	1.0	2.5		mA	V _{OUT} =0.4 V
15	Output high (source) current	I _{OH}	0.4	0.8		mA	V _{OUT} =4.6 V
16	V _{Ref} output voltage	V _{Ref}	2.3	2.5	2.7	V	No load, V _{DD} = 5.0V
	V _{Ref} output resistance	R _{OR}		1		kΩ	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

Characteristics		Sym	Min	Typ [‡]	Max	Units	Test Conditions
1	Input leakage current	I _{IN}			100	nA	V _{SS} ≤ V _{IN} ≤ V _{DD}
2	Input resistance	R _{IN}	10			MΩ	
3	Input offset voltage	V _{OS}			25	mV	
4	Power supply rejection	PSRR	50			dB	1 kHz
5	Common mode rejection	CMRR	40			dB	0.75 V ≤ V _{IN} ≤ 4.25 V biased at V _{Ref} = 2.5 V
6	DC open loop voltage gain	A _{VOL}	32			dB	
7	Unity gain bandwidth	f _c	0.30			MHz	
8	Output voltage swing	V _O	4.0			V _{pp}	Load ≥ 100 kΩ to V _{SS} @ GS
9	Maximum capacitive load (GS)	C _L			100	pF	
10	Resistive load (GS)	R _L			50	kΩ	
11	Common mode range	V _{CM}	2.5			V _{pp}	No Load

MT8870D AC Electrical Characteristics

- V_{DD}=5.0V ±5%, V_{SS}=0V, -40°C ≤ T_O ≤ +85°C, using Test Circuit shown in Figure 10.

Characteristics		Sym	Min	Typ [‡]	Max	Units	Notes*
1	Valid input signal levels (each tone of composite signal)		-29		+1	dBm	1,2,3,5,6,9
			27.5		869	mV _{RMS}	1,2,3,5,6,9
					8	dB	2,3,6,9,12
2	Negative twist accept				8	dB	2,3,6,9,12
3	Positive twist accept						
4	Frequency deviation accept		±1.5% ± 2 Hz				2,3,5,9
5	Frequency deviation reject		±3.5%				2,3,5,9
6	Third tone tolerance			-16		dB	2,3,4,5,9,10
7	Noise tolerance			-12		dB	2,3,4,5,7,9,10
8	Dial tone tolerance			+22		dB	2,3,4,5,8,9,11

‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.

*NOTES

1. dBm= decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of all DTMF tones.
3. Tone duration= 40 ms, tone pause= 40 ms.
4. Signal condition consists of nominal DTMF frequencies.
5. Both tones in composite signal have an equal amplitude.
6. Tone pair is deviated by ±1.5 % ± 2 Hz.
7. Bandwidth limited (3 kHz) Gaussian noise.
8. The precise dial tone frequencies are (350 Hz and 440 Hz) ± 2 %.
9. For an error rate of better than 1 in 10,000.
10. Referenced to lowest level frequency component in DTMF signal.
11. Referenced to the minimum valid accept level.
12. Guaranteed by design and characterization.

	Characteristics	Sym	Min	Typ [‡]	Max	Units	Notes*
1	Valid input signal levels (each tone of composite signal)		-31 21.8		+1 869	dBm mV _{RMS}	Tested at V _{DD} =5.0V 1,2,3,5,6,9
2	Input Signal Level Reject		-37 10.9			dBm mV _{RMS}	Tested at V _{DD} =5.0V 1,2,3,5,6,9
3	Negative twist accept				8	dB	2,3,6,9,13
4	Positive twist accept				8	dB	2,3,6,9,13
5	Frequency deviation accept		±1.5%± 2 Hz				2,3,5,9
6	Frequency deviation reject		±3.5%				2,3,5,9
7	Third zone tolerance			-18.5		dB	2,3,4,5,9,12
8	Noise tolerance			-12		dB	2,3,4,5,7,9,10
9	Dial tone tolerance			+22		dB	2,3,4,5,8,9,11

‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.

*NOTES

1. dBm= decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of all DTMF tones.
3. Tone duration= 40 ms, tone pause= 40 ms.
4. Signal condition consists of nominal DTMF frequencies.
5. Both tones in composite signal have an equal amplitude.
6. Tone pair is deviated by ±1.5 %± 2 Hz.
7. Bandwidth limited (3 kHz) Gaussian noise.
8. The precise dial tone frequencies are (350 Hz and 440 Hz) ± 2 %.
9. For an error rate of better than 1 in 10,000.
10. Referenced to lowest level frequency component in DTMF signal.
11. Referenced to the minimum valid accept level.
12. Referenced to Fig. 10 input DTMF tone level at -25dBm (-28dBm at GS Pin) interference frequency range between 480-3400Hz.
13. Guaranteed by design and characterization.

1		Tone present detect time	tDP	5				
2	T	Tone absent detect time	tDA	0.5				
3	I M	Tone duration accept	tREC					≤ +85°C , using Test Circuit shown in Figure 10.
4	I N	Tone duration reject	tREC	20	Typ [‡]	Max	Units	Conditions
5	G	Interdigit pause accept	tID		11	14	ms	Note 1
6		Interdigit pause reject	tDO	20	4	8.5	ms	Note 1
7		Propagation delay (St to Q)	tPQ			40	ms	Note 2
8	O	Propagation delay (St to StD)	t PStD				ms	Note 2
9	U T	Output data set up (Q to StD)	t QStD			40	ms	Note 2
10	P U	Propagation delay (TOE to Q ENABLE)	tPTE				ms	Note 2
11	T S	Propagation delay (TOE to Q DISABLE)	tPTD		8	11	μs	TOE=V _{DD}
					12	16	μs	TOE=V _{DD}
12	P D	Power-up time	tPU		3.4		μs	TOE=V _{DD}
13	w N	Power-down time	tPD		50		ns	load of 10 kΩ, 50 pF
14		Crystal/clock frequency	fc	3.5759	300		ns	load of 10 kΩ, 50 pF
15	C L	Clock input rise time	t LHCL		30		ms	Note 3
16	O	Clock input fall time	t HLCL		20		ms	
17	C K	Clock input duty cycle	DC _{CL}	40				
18		Capacitive load (OSC2)	CLO		3.5795	3.5831	MHz	
						110	ns	Ext. clock
						110	ns	Ext. clock
					50	60	%	Ext. clock
						30	pF	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

***NOTES:**

1. Used for guard-time calculation purposes only.
2. These, user adjustable parameters, are not device specifications. The adjustable settings of these minimums and maximums are recommendations based upon network requirements.
3. With valid tone present at input, t_{PU} equals time from PDWN going low until ESt going high.

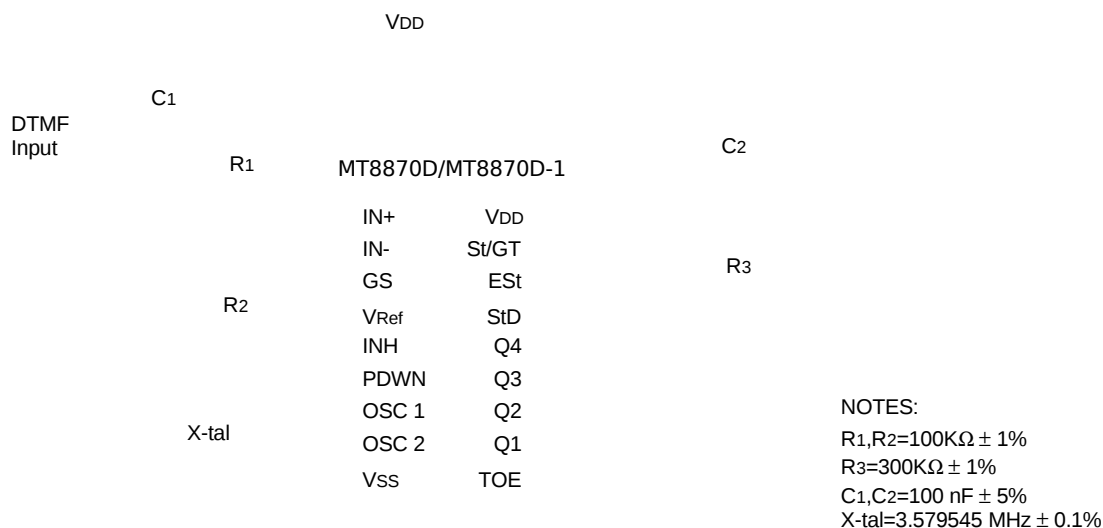
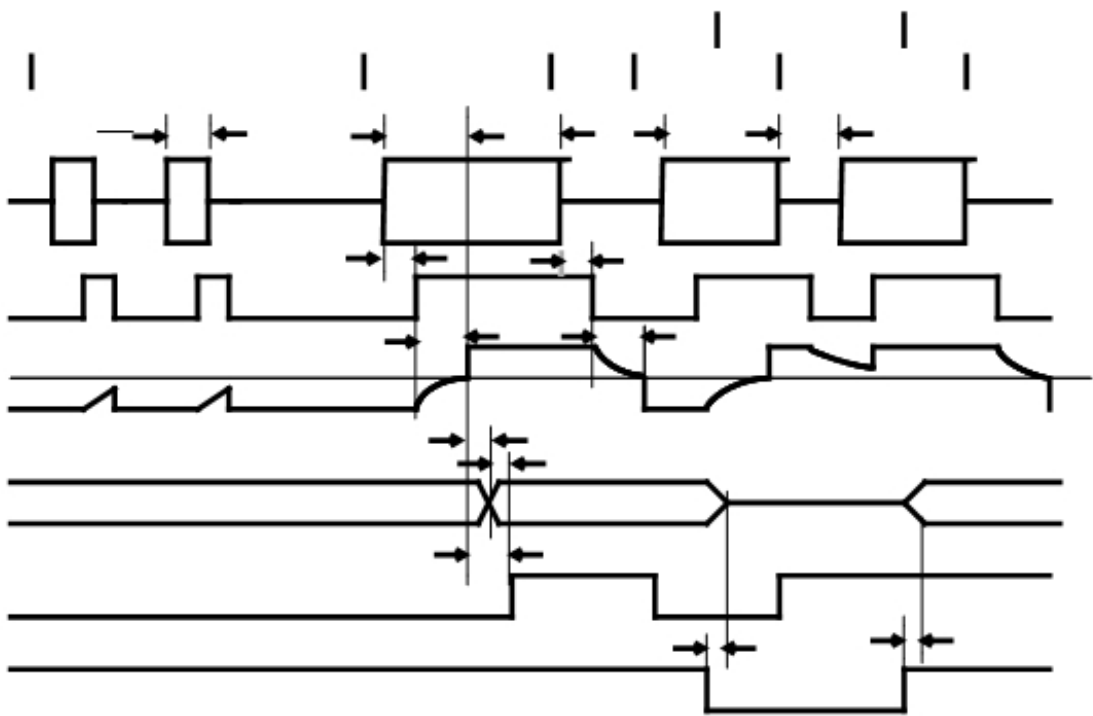
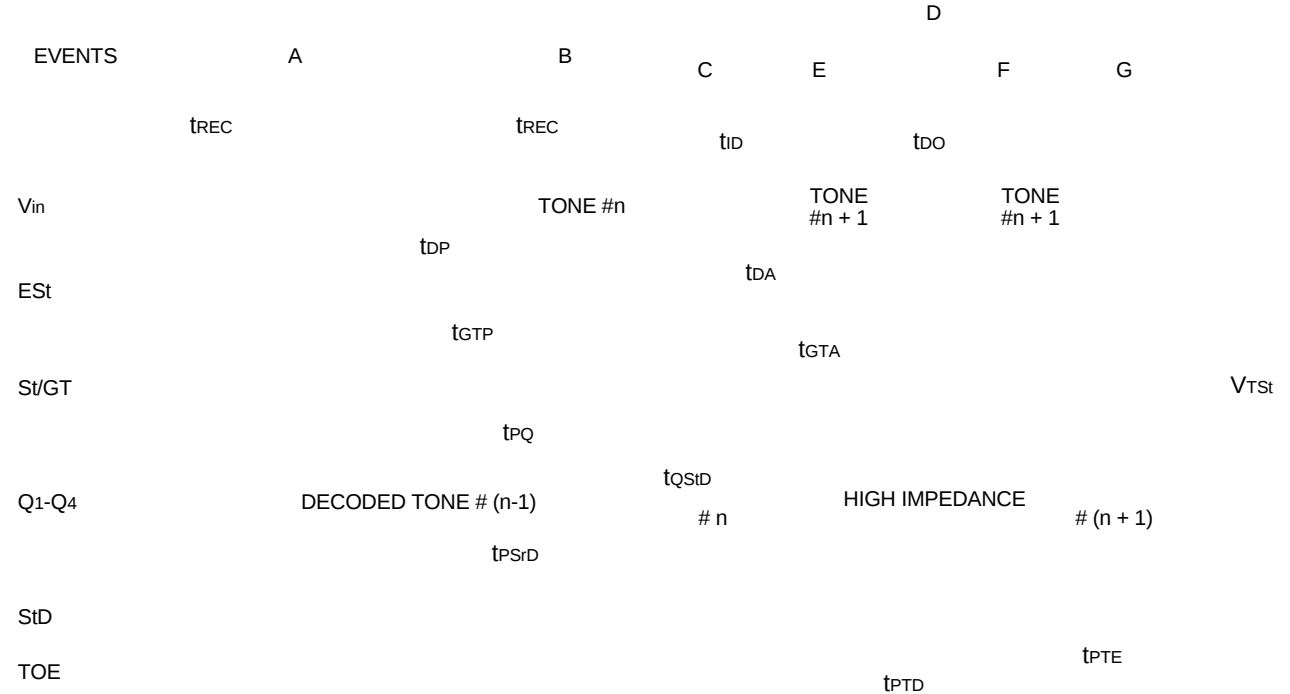


Figure 10 - Single-Ended Input Configuration





EXPLANATION OF EVENTS

- A) TONE BURSTS DETECTED, TONE DURATION INVALID, OUTPUTS NOT UPDATED.
- B) TONE #n DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN OUTPUTS
- C) END OF TONE #n DETECTED, TONE ABSENT DURATION VALID, OUTPUTS REMIAN LATCHED UNTIL NEXT VALID TONE.
- D) OUTPUTS SWITCHED TO HIGH IMPEDANCE STATE.
- E) TONE #n + 1 DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN OUTPUTS (CURRENTLY HIGH IMPEDANCE).
- F) ACCEPTABLE DROPOUT OF TONE #n + 1, TONE ABSENT DURATION INVALID, OUTPUTS REMAIN LATCHED.
- G) END OF TONE #n + 1 DETECTED, TONE ABSENT DURATION VALID, OUTPUTS REMAIN LATCHED UNTIL NEXT VALID TONE.

EXPLANATION OF SYMBOLS

- V_{in} DTMF COMPOSITE INPUT SIGNAL.
- ESt EARLY STEERING OUTPUT. INDICATES DETECTION OF VALID TONE FREQUENCIES.
- St/GT STEERING INPUT/GUARD TIME OUTPUT. DRIVES EXTERNAL RC TIMING CIRCUIT.
- $Q1-Q4$ 4-BIT DECODED TONE OUTPUT.
- StD DELAYED STEERING OUTPUT. INDICATES THAT VALID FREQUENCIES HAVE BEEN PRESENT/ABSENT FOR THE REQUIRED GUARD TIME THUS CONSTITUTING A VALID SIGNAL.
- TOE TONE OUTPUT ENABLE (INPUT). A LOW LEVEL SHIFTS $Q1-Q4$ TO ITS HIGH IMPEDANCE STATE.
- t_{REC} MAXIMUM DTMF SIGNAL DURATION NOT DETECED AS VALID
- t_{REC} MINIMUM DTMF SIGNAL DURATION REQUIRED FOR VALID RECOGNITION
- t_{ID} MAXIMUM TIME BETWEEN VALID DTMF SIGNALS.
- t_{DO} MAXIMUM ALLOWABLE DROP OUT DURING VALID DTMF SIGNAL.
- t_{DP} TIME TO DETECT THE PRESENCE OF VALID DTMF SIGNALS.
- t_{DA} TIME TO DETECT THE ABSENCE OF VALID DTMF SIGNALS.
- t_{GTP} GUARD TIME, TONE PRESENT.
- t_{GTa} GUARD TIME, TONE ABSENT.

Figure 11 - Timing Diagram

